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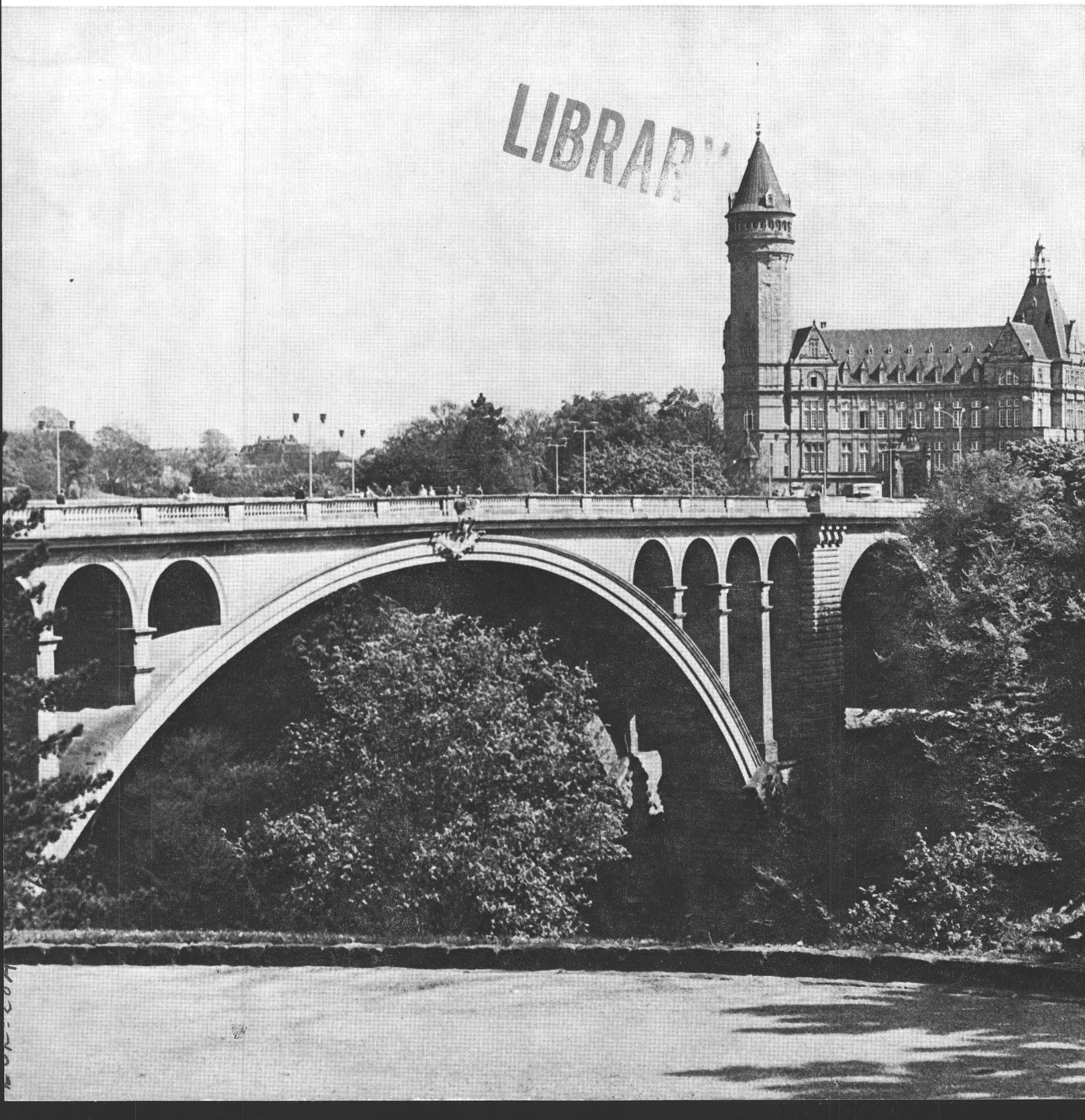

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* ***DEADLINES FOR SUBMISSION*** **(issue No. 14)**
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On the cover: "Pont Adolphe" in Luxemburg: The 1st International Symposium on CAMAC in Real-Time Computer Applications took place in Luxemburg, in December 1973 (Cliché CEC).

CAMAC
bulletin

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Production Editor:

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Correspondence to:

the Secretary of the
ESONE Committee
New provisional address:
H. Meyer, CBNM EURATOM
B-2440 Geel, Belgium

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AN INTRODUCTION TO CAMAC

THE CAMAC SERIAL HIGHWAY — A FUNCTIONAL VIEW

by

D.L. Abbott

Zentrallabor für Elektronik, KFA, Jülich, Germany

(at present: STANDARD ENGINEERING Corp., FREMONT, CALIFORNIA, U.S.A.)

Received 12th November 1974

SUMMARY This paper describes the Serial Highway in terms of the fundamental design parameters of serial systems, such as synchronization and message structure. It is shown that potential applications include non-CAMAC as well as CAMAC environments.

INTRODUCTION

There is increasing interest in the use of serial data transmission for all types of real-time data acquisition and control systems. This is motivated by the increasing size and complexity of such systems, where the cost and complexity of interconnection becomes a major problem. At the same time the development of low cost minicomputers and microprocessors makes it more and more practical to distribute the control in large systems, which also favors serial interconnection. As a result, a number of national and international groups are working on the definition of 'standardized' serial transmission systems for use in industrial and scientific applications.

The CAMAC Serial Highway[1–3] is the product of one of these standardization efforts. In particular, it is a means of interconnecting a large number of CAMAC crates in applications where long distances, ease of interconnection and/or noisy operating environment are important factors. Although it was specifically designed to complement CAMAC instrumentation, its functional characteristics are by no means defined by or limited to CAMAC[4]. In order to promote better understanding of the Serial Highway and fuller appreciation of its potential range of application, this paper describes the Serial Highway in terms of the fundamental design parameters of serial systems. The aim is to emphasize the generality of this particular solution and thereby promote its application to non-CAMAC as well as CAMAC environments.

SERIAL TRANSMISSION IN REAL-TIME SYSTEMS

To begin with, what do we mean by 'serial' data transfer? Any interface is serial to some degree. The CAMAC Dataway, for example, transfers one 24-bit word per cycle. Thus multiple words are transferred serially on the Dataway. However, when one speaks of a serial transmission system, this is usually understood to mean one bit at a time or bit-serial. It is further understood to be a connection consisting only of a data line and possibly a timing, or clock, line. Specifically, there are no special addressing and control lines such as N, A, F, S1, etc. Address and control information share the same line as data and must somehow be separated from data and interpreted by the receiving device. Operations in such a system consist of a series of bits or bytes constituting self-contained 'messages' holding all of the information necessary to carry out the required action or data transfer.

This definition is not necessarily restricted to bit-serial operation and in fact the Serial Highway offers a bit-parallel, byte-serial mode for high data rate requirements. By the definition this is still a serial system because address and control information share the same lines as the data.

The Serial Highway was designed to satisfy a number of requirements, some of them seemingly contradictory. As a way of providing simple, cheap CAMAC computer interfacing, the Serial Highway should be compatible with the most universal interface of all, the Teletype port. At the other end of the performance spectrum, it should be capable of data rates comparable with those on the Branch Highway. In either case, the real-time nature of most CAMAC installations implies the need for relatively fast response time on the Highway. The Serial Crate Controller should be kept as simple as possible, with 'dumb' hardwired logic. This has important consequences for the message format and also implies a hierarchical structure wherein all system control resides in a more intelligent system driver.

DESIGN PARAMETERS OF SERIAL SYSTEMS

Configuration

Fundamentally, the Serial Highway is a unidirectional loop originating at the output port of the loop controller, called the Serial Driver, passing

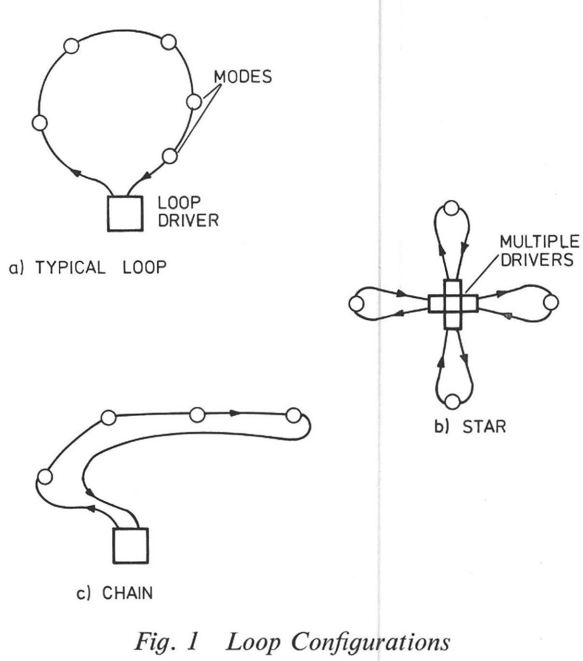


Fig. 1 Loop Configurations

in succession through each Serial Crate Controller, or more generally 'node', and terminating at the input port of the Serial Driver (Fig. 1a). Up to 62 nodes may be inserted in the loop. Normally, nodes are transparent to the loop, repeating at their output ports what they receive at their input ports. However, when a node is involved in a transaction, it may interrupt the loop and insert its own information in place of the incoming bytes.

Each node, and Serial Driver, has one input and one output 'D port' whose characteristics are defined in the specification. Data and clock signals at the D ports are carried on separate wire pairs with balanced transmitters and differential receivers. Both bit-serial and byte-serial modes of operation are provided. In bit-serial mode, data is transferred one bit at a time on one pair of wires accompanied by a bit clock on another pair. In byte-serial mode, data is transferred eight bits at a time on eight pairs accompanied by a byte clock on a ninth pair (Fig. 2).

The communication links between nodes are left

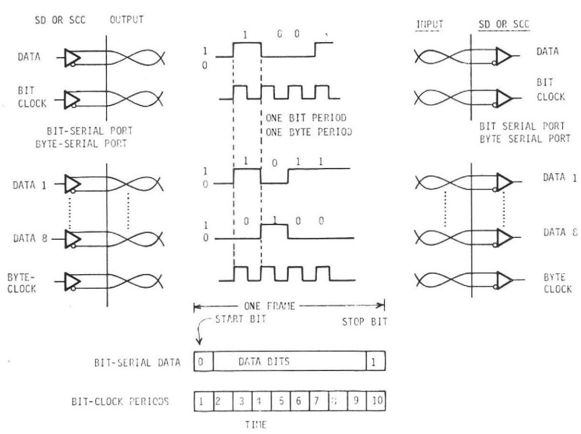


Fig. 2 D-Port Data Format and Signal Standards

undefined except to note that timing information must accompany the data. D ports may be connected directly, typically using 100 ohm dedicated twisted pairs. Alternatively, other media such as telephone circuits, coaxial cable, and microwave may be used with the appropriate modulation technique and interface to the D port. Such links are called 'U ports' (U for undefined).

The uni-directional loop can be the basis for other configurations. For example, a set of loops, each with a Serial Driver and only one node, forms a 'star' (Fig. 1b). Although it requires more hardware (multiple drivers), the star is useful where the data rate of a shared loop is insufficient or where very flexible node-to-node communication is desired. Another variation of the loop, called a 'chain', results when the return link from the last node to the Serial Driver input is 'folded back' to folllow the same physical path as the outgoing links (Fig. 1c). Although this may increase the total length of the loop, it provides better utilization of typical full-duplex communication channels such as modems.

Synchronization

The synchronization of bits, bytes and messages on a serial link provides timing information equivalent to the explicit timing lines of conventional I/O busses, e.g. BUSY, S1, S2. Like error detection, synchronization necessarily imposes a certain amount of redundancy, or 'overhead', on the data transfer. The degree of synchronizing redundancy, and the form that it takes are among the principal distinguishing characteristics of serial systems.

Synchronization occurs at three levels: bit, byte and message.

Bit synchronism. In a bit-serial system the receiving node must somehow be informed by the transmitting node precisely when to strobe the incoming bits into its input register. One way is for the transmitter and receiver to agree in advance on what the data rate will be. Then if the receiver is able to detect the beginning of a bit stream, i.e. the leading edge of the first bit, it can strobe its register in the middle of each bit, relying on the transmitter to maintain the pre-arranged data rate.

The number of bits that can be transmitted, before resynchronization is necessary, is limited by the relative accuracy of the clock frequencies at the transmitter and receiver. If, for example, the two clocks are within $\pm 5\%$ of each other, then after ten bit periods the receiving clock may have drifted by half a bit period relative to the transmitting clock, and will be out of synchronization. Consequently, this 'asynchronous' mode is generally restricted to low-speed data terminals.

The more common practice in data communication systems, including the Serial Highway, is to have the transmitter send a 'bit clock' together with the data, to strobe the data into the receiver's register. The clock may be sent on a separate line or combined with data on one line using an appropriate modulation technique. This form is called 'synchronous' transmission. The data rate is determined entirely by the transmitter, within limits imposed by the transmission medium. The receivers are thus said to be 'data rate independent'.

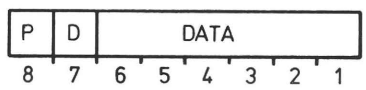
Byte Synchronism. Bits are normally organized into groups called bytes, usually 8 bits per byte. This is the basic unit of information in most systems. Byte synchronism consists of identifying the boundaries between bytes, often called byte 'framing'. If the receiver can depend on the bytes being contiguous, with no gaps between them, and if it can somehow detect the beginning of the first byte, then it simply counts off the correct number of bits, eight for example, to find the start of the second and each successive byte. Between messages the transmitter sends a series of 'synchronization bytes', with a special bit pattern which enables the receiver to 'get in sync' and correctly identify the beginning of a byte. This form is used for data transmission systems involving large blocks of data sent at high speed.

As an alternative to the above, each byte may carry its own framing information in the form of 'start' and 'stop' bits. An eight-bit data byte is embedded in a ten-bit frame consisting of a start bit which is logic zero, followed by the eight data bits, followed by a stop bit which is logic one (Fig. 2). The receiver recognizes the start of a byte by the 1 to 0 transition of the leading edge of the start bit. Since the bytes carry their own framing information, they need not be contiguous. This form is used for the Serial Highway because it is simpler to implement in hardware and is compatible with the terminal port of any minicomputer. In low speed applications one or two MOS-LSI chips can handle the entire serial-to-parallel and parallel-to-serial conversion process.

The result of the byte synchronizing process is to derive a 'byte clock' which indicates to the receiving node that a complete byte has been assembled and is ready for processing. In the byte-serial mode, the byte clock accompanies the eight bits of data on a ninth signal line and is thus equivalent to the bit clock in the bit serial mode.

Message Synchronism. As its name implies, message synchronization consists of correctly determining the boundaries between messages. The techniques normally used in data communications are not well suited to the Serial Highway because they add considerable overhead both in time and in hardware to the handling of short control messages characteristic of real-time systems.

All bytes on the Serial Highway are formatted as shown in Fig. 3. Six bits of every byte are for information, bit 7 is used as a 'delimiter' indication



D = DELIMITER BIT
P = ODD PARITY OVER BITS 1 TO 7

Fig. 3 Serial Highway Byte Format

and bit 8 is odd parity over the other seven. All bytes within a message have bit 7 at logic 0. The last byte of a message and all subsequent bytes up to the beginning of the next message are called 'delimiter bytes' and have bit 7 set to 1. Thus the beginning of a message is defined as the first non-delimiter byte following a sequence of one or more delimiters. Likewise, the end of a message is defined as the first delimiter following a sequence of one or more non-delimiters.

Message synchronization is thus accomplished by inspecting one bit in every byte, a task easily done in hardware. An apparent disadvantage is the six-bit data field. Since most computers operate on eight-bit bytes, this necessitates some repacking of data. At the Serial Driver the data packing and unpacking can be done by software or hardware. The software overhead for data packing is not significantly greater than that needed for message synchronization in some other systems. For short messages, this technique requires fewer bytes than a conventional data communications format.

Error Detection

Serial systems are often used under conditions which expose the message to error-inducing noise. To guard against the possibility that corrupted messages may be acted upon, error detection and handling schemes are usually included in the design of serial systems. Like synchronization, error detection is accomplished by adding systematic redundancy to the transmitted data.

The Serial Highway uses a Geometric Error Detection Code which provides a significant reduction in the probability of undetected errors over the intrinsic error rate of the communications channel. This is a two-dimensional code where each byte contains an odd-parity bit, and the message ends with a checksum byte containing the modulo-2 sum (even-parity) of all the bytes in the message.

In addition to its excellent performance, the Geometric Code is much simpler to generate than other well-known codes such as the cyclic redundancy check, especially for byte-serial operation.

Upon receiving a message with an error, a receiver node takes no action on it except to send an error reply back to the transmitter, which then repeats the message. In most cases, there is a high probability that the repeated message will be received error free. This is known as ARQ and is the simplest, most widely used form of error correction.

Message Structure and Protocol

All messages on the Serial Highway fall into one of three categories: Command, Reply and Demand. A Command Message is directed from the Serial Driver to a loop node and specifies some action to be performed in the node. It may also contain data for a write command.

A Reply Message is directed from a loop node to the Serial Driver and is always in response to a Command Message. The Reply describes the state of the system after carrying out the action specified in the command or, alternatively, indicates that the command was not executed due to a transmission error. It may also carry data in response to a read command.

A Demand Message is also directed from a node to the Serial Driver. It is generated spontaneously by a node to indicate a request for service. When the node is a CAMAC crate for example, the Demand is in response to a LAM signal. The Demand message contains information relating to the nature of the request.

Each node on the loop has a unique 6-bit address to which messages are directed, or from which messages originate. It is fundamental to the operation of the loop that the first byte of any message be a node address. For a Command message, this will be the address to which it is directed. For a Reply or Demand message, it will be the address from which it originated. Following the node address is the control and/or data portion, conveying the information content of the message. Following the information field comes a checksum byte which, for Reply and Demand messages, may be combined with the Delimiter byte in which case it is called the ENDSUM byte.

Command-Reply Sequence. Because the loop is unidirectional the Command message must provide space in which the addressed node can insert its Reply after it has executed the message. This is called the Reply space and consists of non-delimiter bytes which normally convey no information. It must contain at least as many bytes as the expected Reply message plus enough bytes to fill the time needed to execute the command. A specific SPACE byte is defined in the specification but, in principle, any non-delimiter byte may be used. The Reply Space is terminated by a delimiter, called the END byte, which terminates the Command-Reply sequence.

Demand Sequencing. Demand messages may be inserted in the loop between other messages, thereby replacing the inter-message delimiter bytes (called WAIT bytes). Demand message initiation is enabled in a node by the receipt and retransmission of a delimiter (END or ENDSUM). The delimiter that enables a node to insert a Demand in the message stream may be followed immediately by Type L defined in the specification. The bit fields labeled SC, SA, SF, SN, SW, SR, SQ, SX, and SGL correspond to the Crate address and the Dataway signals A, F, N, W, R, Q, X and LAM respectively. M1 and M2 are message identification bits required at the Serial Driver input. The P and E fields are elements of the Geometric Error Code. The Reply status bits ERR and DERR (Delayed ERR) indicate whether or not the current Command and previous Command, respectively, successfully accessed the required CAMAC address.

The SGL field is a binary number identifying the type or source of the Demand or the action required. It may be derived from the L signals on the Dataway by any process of selection, grouping, priority encoding, etc., performed either by the SCC or by a separate SGL encoder connected to the SCC.

EXTENSIONS OF THE SERIAL HIGHWAY

The basic structure and operating principles of the Serial Highway as outlined above provide a great deal of flexibility in tailoring message formats to suit particular applications, while still maintaining compatibility with the CAMAC message structure non-delimiter bytes of a new incoming message. Therefore, the node must buffer incoming information (non-delimiter) bytes until it has completed its demand transmission. This delay buffer acts like a first-in-first-out queue (FIFO) and remains in the loop until emptied by the arrival of WAIT bytes. The buffer capacity must equal the length of the longest Demand message generated by the node.

CAMAC Message Structure. Fig. 4 shows how the rules of message formatting are applied to a hardwired CAMAC crate controller such as the defined by the specification and used by standard CAMAC nodes within the same system. The information field may be of any length and any format appropriate to a particular node. Minimal compatibility with standard Serial Drivers, either in hardware or in software, does suggest that the message identifier bits be retained in all messages and that the ERR bit of the Reply status byte also

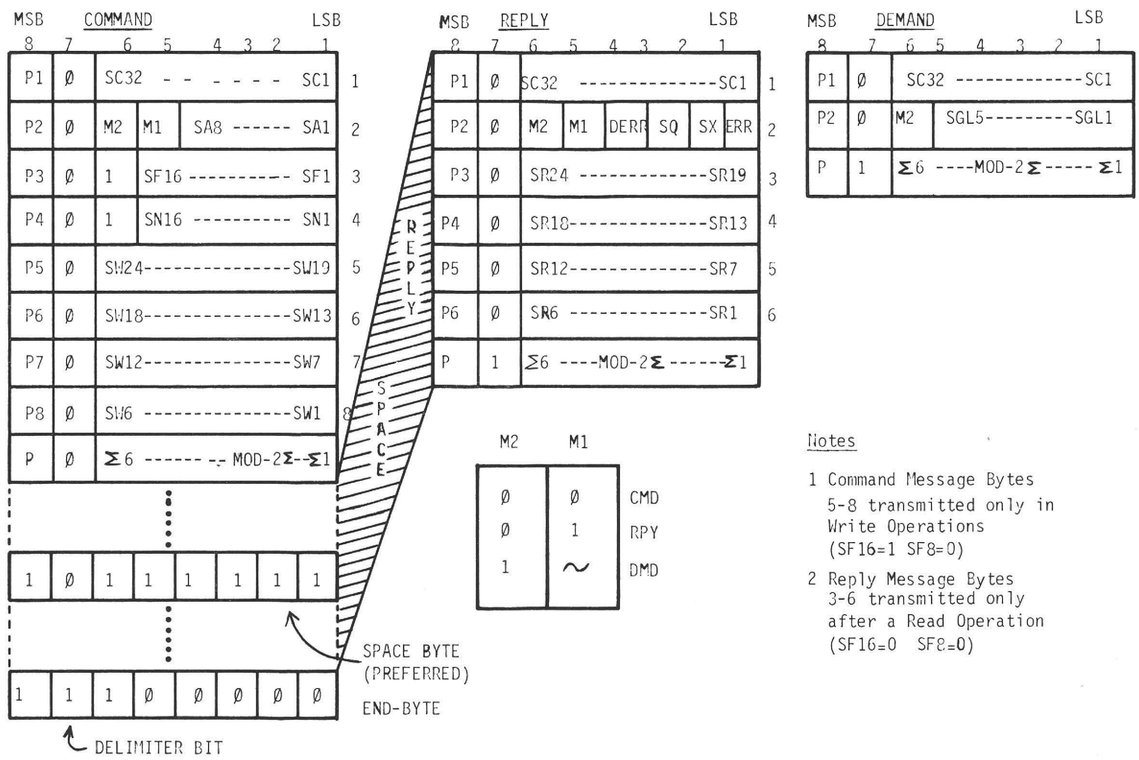


Fig. 4 CAMAC Message Formats on the Serial Highway

be retained. However this is not strictly necessary.

Already work is under way on extended uses of the Serial Highway. These uses extend in two directions, up and down, from the defined message structure.

Terminal and Instrument Interfacing

Some potential applications of serial transmission systems do not require an expensive CAMAC crate at every node. It is therefore useful to consider interfacing individual instruments, or even data terminals, directly to the Serial Highway. This resembles the Hewlett Packard Instrument Bus but without the limitation to either 15 instruments an overall length of 15 meters.

Messages in this type of environment would tend to be simpler and shorter than the CAMAC format since less function and addressing information is required. It should be possible to define a fairly general 'Interface Control Unit' for connection to the Serial Highway. A few TTL or MOS chips should be sufficient and the whole unit could be supplied as an encapsulated module.

Intelligent Node Controllers

Serial crate controllers have already been built utilizing micro-processors[5]. This approach reduces response time and traffic on the highway by servicing LAMs and preprocessing data within the crate. Intelligent nodes reduce the need for CAMAC command messages in favor of more efficient block-structured messages transferring perhaps 64 bytes of data per message. In this case, the defined CAMAC message structure is highly inefficient requiring twelve bytes to transfer four bytes of data. Block structured messages could also be implemented in hardwired controllers[6].

A system with intelligent nodes can operate with slower communication channels than one with passive controllers. Furthermore each node has a high degree of autonomy, allowing it to continue operating in a degraded mode if the loop is broken.

Additional Possibilities. Multicrate addressing is under investigation[7], to provide a means whereby several crates (or nodes) could be referenced simultaneously by the same command message. A variation of this is a Demand Poll message which would eliminate the need for a delay buffer by periodically polling all nodes for demands. In some cases, this could result in significant simplification by putting demand generation entirely under control of the Serial Driver.

Normally, all transfers on the Serial Highway are between the Serial Driver and a node. With intelligent node controllers, however, it may be useful to provide a direct node-to-node transfer mechanism. This is being studied, and raises questions about the nature of the Serial Driver. Fundamentally, each loop has only one Serial Driver. In principle, however any device connected to the loop could be permitted to assume the role of driver, subject to the restriction that, at any time, there must be only one active driver.

CONCLUSION

As CAMAC expands into non-nuclear areas, there is a need for flexibility in the face of new requirements and design parameters. Although the Serial Highway was developed specifically for CAMAC and with only one message structure in mind, it has been shown to be an extremely versatile mechanism for serial data transmission in real-time control environments. As experience in using the Serial Highway accumulates, generally useful message structures covering various applications and special requirements should emerge. This kind of flexibility can have a very positive influence on the further development and application of CAMAC.

ACKNOWLEDGEMENT

The ideas presented in this paper are the personal opinions of the author, although this view of the Serial Highway was developed by the Serial System Compatibility Sub-group of the ESONE Dataway Working Group. The work and contributions of members of the sub-group, and others interested in broader applications of the Serial Highway, are gratefully acknowledged.

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APPLICATION NOTES

1 A CAMAC APPLICATION IN THE QUALITY CONTROL OF HIGH TEMPERATURE REACTOR FUEL

by

W. Attwenger and F. Buschbeck

Elektronik-Institut, Forschungszentrum, Seibersdorf, Austria

Received 12th November 1974

SUMMARY Special measuring systems using CAMAC have been disigned for on-line quality control during the production of coated fuel particles for high temperature nuclear reactors.

INTRODUCTION

The growing demand for energy at high temperature levels forced the development of the High Temperature Gas-Cooled Reactor (HTR)[1]. HTR nuclear power stations, now coming into commercial use, operate with outlet-temperatures of the cooling gas (Helium) up to 800°C. Prototype reactors have reached up to 950°C in continuous operation, and temperatures over 1000°C are envisaged in the future.

Due to temperature and neutron-economy, only graphite can be used as the core construction material. Unfortunately graphite is penetrated easily by some of the fission products. To overcome this difficulty a new fuel concept, the coated particle, was developed. By this concept the fuel (UO_2, UC_2) is divided into small spherical particles of 400-800 μ diameter, which are coated with different layers of pyrocarbon (PyC) and silicon carbide (SiC). Each of these layers, with a thickness up to 100 μ, has a special function. The innermost is PyC of very porous structure and acts as a buffer and reservoir for fission gases, most of which are radioactive. The next layer is high density isotropic PyC retaining practically all of the fission products. The few exceptions are retained by the following SiC layer. The outermost layer is again high density isotropic PyC, acting primarily as a pressure vessel. Thus a coated particle can be thought of ds a 'mini fuel element'. The actual HTR fuel element is formed by pressing a mixture of graphite powder and coated particles into different shapes, depending on the specific core construction.

While the fuel kernels are produced by several methods, only the fluidized bed technique is used for production of the coated layers. By this technique the fuel kernels are fluidized in a vertical heated tube by gas entering at the bottom of the tube. The different coating layers are formed by introducing reaction gases such as hydrocarbons or silanes and by varying the temperature, gas flow and gas composition.

It is evident that the required properties of the different layers are closely connected with deposition rate, thickness and structure. Methods for rapid measurement of diameter, thickness and anisotropy were developed to meet the demand for on-line control.

PARTICLE DIAMETER AND LAYER THICKNESS

An easily-handled, fast and accurate method is required for the on-line determination of particle diameter and layer thickness during production. A recently developed opto-electronic measuring system, based on the shadowing of an illuminated photodiode, meets these demands[2]. The system allows the determination of diameters in the range of 300-1500 μ with an error less than ±2 μ and a feed rate up to 100 particles per second. Particle diameters and layer thicknesses are determined by taking a representative number of kernels (e.g. 10 000), and then making measurements after the deposition of each successive layer. A computer (e.g. PDP-8/e), linked to the system via CAMAC, stores the data, calculates the number of measured particles, their mean diameter, mean layer thickness and the corresponding standard deviation. The density of a layer can be determined with sufficient accuracy from the calculated mean volume of the layer and the weight increase. A display, a plotter, and a teletype attached to the computer allow fast data feed-back to production, as well as documentation.

Method of Measurement

A parallel homogeneous light beam illuminates a photodiode via a narrow parallel slit. The beam is partially interrupted by the measured particle. The reduction of the light current, which is measured by the photosensitive diode, is proportional to the particle diameter. As the slit-width cannot be made indefinitely small, a correction is made by the computer for those particles having a diameter comparable with the slit width. The shadow-pulse duration is in the order of 50 to 150 μs. The light intensity is stabilised to its maximum value, corresponding to the intensity when no particle is in the light beam. The stabilisation is necessary to ensure a stable scale factor. If a particle passes the light beam, the maximum value of the photocurrent reduction is detected by a peak-hold circuit. This value is digitized by means of an ADC-module, and a LAM-signal is generated. Thus, a normal data transfer into the computer is initiated (Fig. 1).

The following elements of the measurement channel are built in into one double-width CAMAC module (KDM), amplifier, peak detector with hold-circuit, ADC, brightness control, timing and LAM-Logic[3].

The opto-mechanical part of the CPA equipment includes the particle feed system, the optical system, a pre-amplifier and the necessary control devices (push buttons and number switches). The push buttons for Calibration Start, Measurement Start and End of Calibration or Measurement cause a LAM to be generated. The data from 10 number switches, for date and charge number, is transferred to the computer by a polling procedure through an external multiplexer. A set of indicator lamps

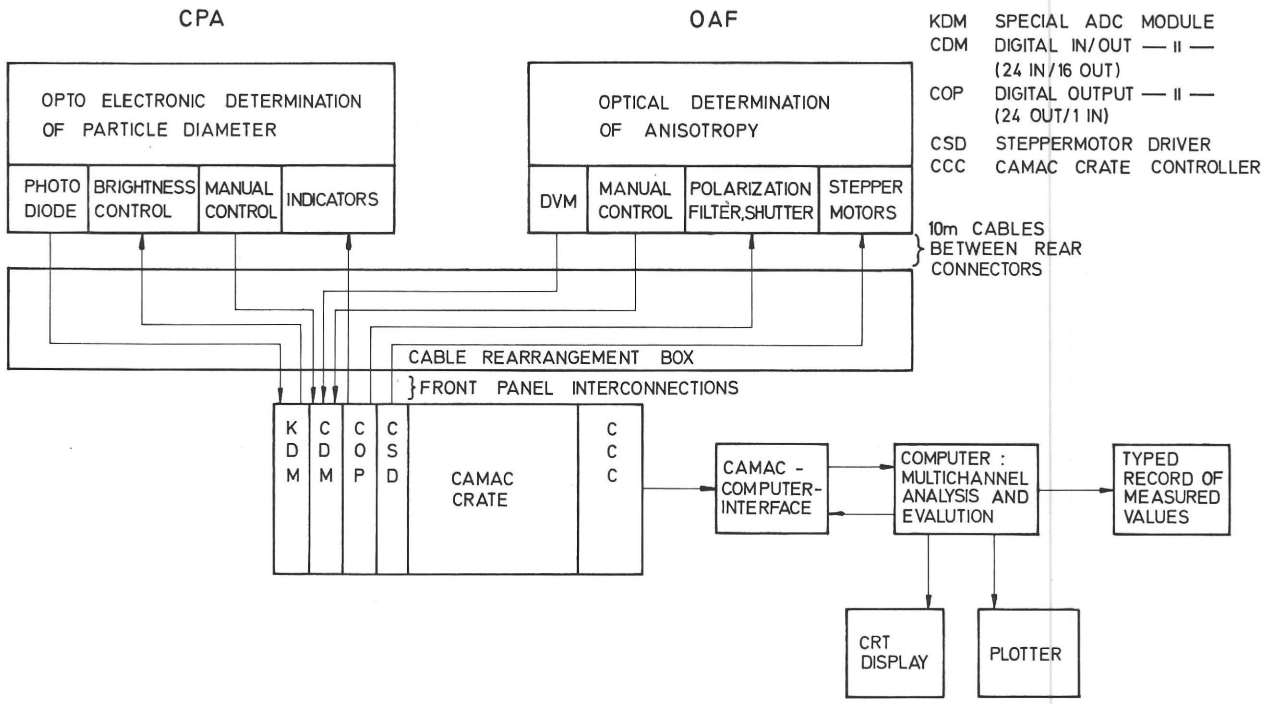

Fig. 1 Block Diagram of the Equipment for the Opto-Electronic Determination of Particle Diameter and Layer Thickness and the Optical Determination of the Anisotropy of Pyrocarbon Coatings

shows the operating mode of the system. The input and output signals are transferred by appropriate CAMAC I/O-modules.

A testing device is built in into the equipment for checking the correct functioning of the optical and detection systems. The calibration is made by means of steel balls with a diameter of $1000\,\mu m \pm 1\,\mu m$ (specified by the supplier). Evaluation software, written in assembly language is available for the PDP-8 with SGAE crate controller CCC-2b and for the PDP-11 with a modified Wenzel crate controller.

ANISOTROPY OF PYROCARBON COATINGS

Materials which consist of anisotropic crystallites show in bulk also more or less anisotropic behaviour, depending on the amount of preferred orientation in the direction examined. Pyrocarbon, with properties somewhere between isotropic coke and highly oriented graphite, can be produced in a wide range of anisotropy. Reactor tests of pyrocarbon-coated particles show a close connection between low anisotropy of a PyC layer and high irradiation stability. This relationship is valid not only for the layer's bulk, but also for local variations or gradients within the layer.

A new method had to be developed to measure such fine detail. The method is based on the difference in reflectivity of an anisotropic material for polarised light, with the polarisation plane parallel or perpendicular to the main axis of anisotropy. The ratio of light reflection by PyC with the plane of polarisation parallel and perpendicular to the direction of deposition is defined as OAF (Optical Anisotropy Factor). The OAF-value is a true measure of anisotropy and in direct correlation to the irradiation stability of PyC. The measurement is carried out on polished metallographic sections of coated particles.

Method of Measurement

The OAF-measuring equipment consists of a modified high-resolution microscope with a microphotometer including a digital voltmeter ($3\frac{1}{2}$ digit). In the incoming light beam there are a polariser and a beam shutter which are operated electromechanically. The motor driven stage allows the sample to be moved in steps of $1\,\mu$. The photometer contains a rotating disc carrying nine different measuring windows which allows selection of the optimum size. The mechanical devices are controlled by CAMAC output modules and a stepper motor driver module. A CAMAC input module monitors the execution of the electromechanical actions. The measuring procedure starts with manual insertion of the prepared sample and determination of the starting point and measuring direction. Then the measuring program is started on the computer. This first measures the reflectivity in one polarisation direction and transfers the digital voltmeter signal reading into the computer by means of CAMAC. Then the plane of polarisation is rotated, and a second measurement of the reflection is made and the data transferred. The shutter is inserted, a measurement of dark current is made and this data is transferred. The computer calculates the OAF-value and the sample is moved to the next position.

ACKNOWLEDGEMENT

We would like to express our sincere thanks to our colleagues in the Institute for Metallurgy and Institute of Electronics for their effective collaboration during the design and construction period and for their support in writing this paper.

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3. Buschbeck, F., Telefont, H., Kugeldickenmeßgerät in CAMAC, KDM-1. SGAE-Bericht Nr. 2225, Januar 1974.

2

A CAMAC-BASED LABORATORY COMPUTER SYSTEM

by

G.P. Westphal

Atominstitut der Österreichischen Hochschulen, Vienna, Austria

Received 28th October 1974

SUMMARY A CAMAC-based laboratory computer network is described. By sharing a common mass memory this offers distinct advantages over slow and core-consuming single-processor installations. A fast compiler-BASIC, with extensions for CAMAC and real-time, provides a convenient means for interactive experiment control.

For the nuclear research centre of the Austrian Universities, which is built around a Triga Mark IV reactor, a laboratory computer network has been developed and partially installed (Fig. 1). It will be completed to the level described in this paper during 1975. The main research activities of the institute are in the fields of pure and applied neutron physics, solid state physics, low energy nuclear physics and nuclear chemistry. Typical data acquisition tasks for a beam tube experiment at the reactor are supervision of neutron count rates, analog multiplexing of transducer outputs, and control of goniometer positions. Further, automatic timing of the experiments and response to alarm conditions has to be provided.

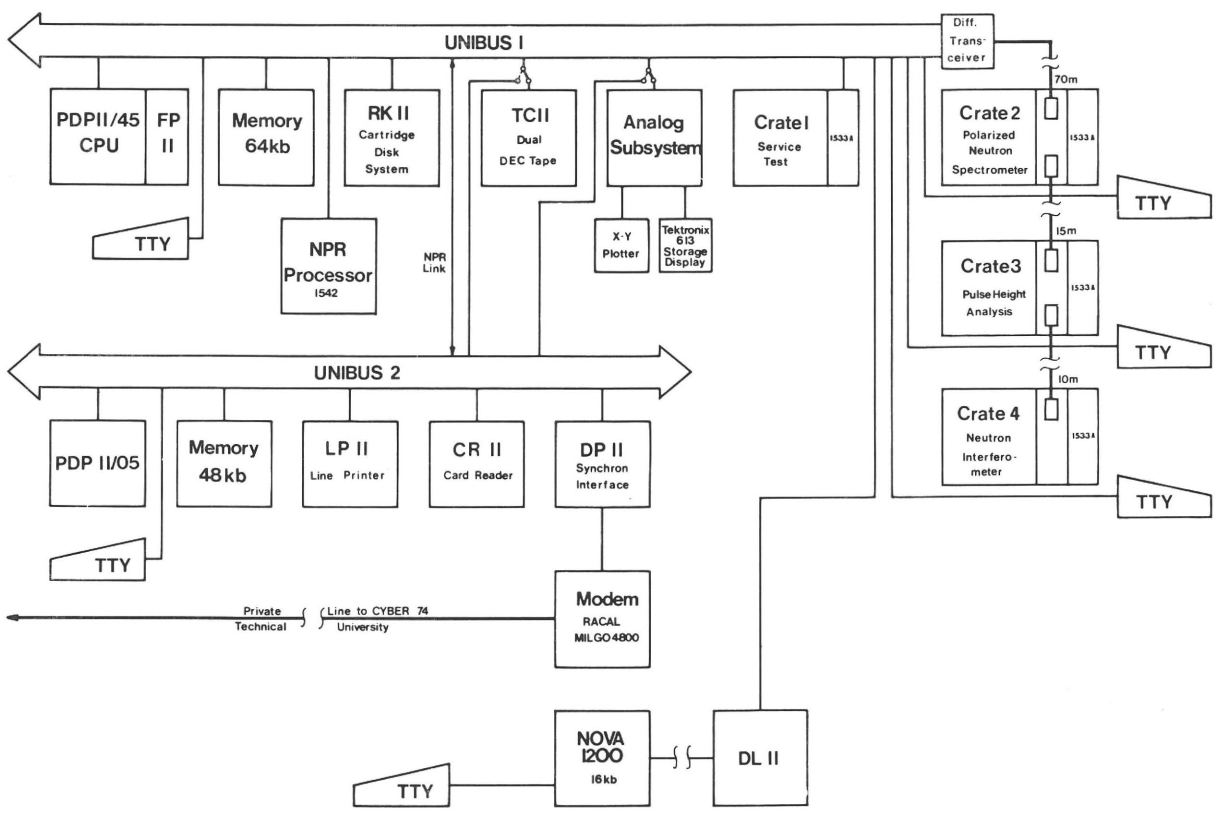

Fig. 1 Laboratory Computer System

INTERACTIVE TERMINALS

Due to the relatively low data rates involved, most of the computer power could be used to support an interactive terminal system programmed in a high level language containing real-time elements. A terminal unit physically and logically consists of one TTY and one or more CAMAC crates interfaced by means of Type U controllers (Borer 1533A) to the differentially extended UNIBUS of a PDP-11/45. The greatest distance from the experimental area to the computer room is 70m. Two terminals located at reactor beam tubes are dedicated to neutron spectrometer control. A third one at the neutron activation analysis facility is for multichannel analysis. A fourth crate, which is for service and testing purposes, is installed in the computer room. The PDP-11/45 is equipped with an RK-05 cartridge disk system, a dual DEC tape drive, a line printer (300 lpm) and a graphics system formed by a storage scope and an X-Y plotter. A disk based system under the real-time executive RT-11 has 24k core for program and 8k core located in high address space as a DMA buffer for multichannel analysis. This DMA buffer is accessed by means of a Borer 1542 DMA control and the analog-to-digital converters are interfaced by means of 128-word buffer registers. The terminals are serviced by a recently-developed multi-user BASIC, which has an incremental (line-by-line) compiler and combines very fast execution with good core economy. Speed is further enhanced by the floating point processor of the PDP-11/45. Complete file handling capability is provided, including CHAIN and OVERLAY statements. A CALL feature allows easy implementation of the CAMAC functions for control of the 1533A, as described by Halling *et al.*[1]. To provide full real-time capabilities a LAM statement has been added, which on LAM gives control to another line of the user's BASIC program.

Example:

150 CALL "LAM" (C, N, STATEMENT NUMBER)

The internal interrupt vector generator of the 1533A control decodes 16LAMs per crate. To provide a means of programming the system's real-time clock, another CALL has been designed, giving control to a BASIC subroutine after a predetermined time.

Example:

250 CALL "TMR" (HOURS, MINUTES, SECONDS, STATEMENT NUMBER)

Up to 64 timer tasks are stored in a dynamically updated table and executed in proper sequence. CALL "TDY" gives time of day. Further CALLs support the graphic system and the multichannel analysis system via the DMA control. Complete error diagnostics have been incorporated into the CALLs, and crates are assigned to users at system start.

COMPUTER NETWORK

Presently the PDP-11/45 is connected to the CDC Cyber 74 central computer of the Technical University by means of a synchronous 4800 baud link and the UT 200 terminal procedure under COMTEX. Being a high priority task, the UT 200 has to be operated in the foreground, which makes concurrent real-time experimental activities ineffective and almost impossible. Therefore, a PDP-11/05 has been purchased as a 'background' processor, which will be linked by an NPR connexion to the 11/45. On the 11/05, which has 24k core, a modified RT-11 monitor will be operated. This believes the NPR link to be its system device. Thus, complete file access to a common mass memory is provided. Program development, line printer service, plotting, spooling and last, but not least, remote job entry to the central computer can be performed on the 'background' processor, while full real-time activity is possible on the 11/45.

Following a similar philosophy of data base sharing, a small 8k NOVA 1200 has already been interfaced to the 11/45. The NOVA, which is used as a non-CAMAC special purpose multichannel analyzer, is linked via a 9600 baud asynchronous connexion to the 11/45 and all programs are loaded by means of an 'interactive' loader from the system disk to the NOVA. Character transfer in the 11/45 is done by a high priority interrupt service routine and imposes a negligible load on the processor. The link is full duplex. Data from the NOVA are written into files, which may be named and opened from the NOVA Teletype.

During 1975 the common data base will be expanded by two additional RK disk drives and a second 11/05 with CAMAC peripherals and 16k core, operating a single-user BASIC, similar to the multi-user BASIC, under RT-11. This computer will be linked to the network by means of an asynchronous 9600 baud connexion, and will be located at the accelerator laboratories approx. 150m from the computer room.

ACKNOWLEDGMENTS

This work is supported by the Science Foundation of the Austrian National Bank under project no. 458.

The author wishes to thank all members of the institute for their contributions to this work, especially Mr. E. Seymann and Mr. H. Großnegger for skilful program development and Mr. K. Jöstl and Mr. P. Schröder for excellent hardware construction.

REFERENCE

1. Halling *et al.*, *CAMAC Bulletin*, No. 6, p. 15.

NEWS

THE DEFINITION OF IML AVAILABLE

IML is a language used to express the operations described in the CAMAC hardware specifications, and their interaction with a computer system. IML statements link CAMAC structures and modes of operation to data structures and real-time features in the computer system.

The definition of IML, contained in the identical documents ESONE/IML/01 (Oct. 74) and TID-26615, is a guide for those implementing languages and operating systems who wish to make CAMAC input/output operations available to users.

Copies of these documents, entitled "The Definition of IML", are now available, on application, from the ESONE Committee (Dr. H. Meyer, CBNM-CRC, Steenweg naar Retie, B-2440 GEEL, Belgium) for ESONE/IML/01 and the U.S.AEC NIM Committee (Mr. L. Costrell, US Dept. of Commerce, National Bureau of Standards, Washington D.C. 20234, USA) for TID-26615.

3

GROUND REPLAY EQUIPMENT FOR THE ALPHA JET CRASH-RECORDER

by
B. Müller and K. Rosenblatt

Dornier System GmbH, Friedrichshafen, Germany

Received 13th January 1975

SUMMARY Two Ground Replay Equipments (GRE) have been developed to read data from the crash-recorder of the Alpha Jet after each flight. The equipment is a mobile station, with recorder replay electronics consisting entirely of standard CAMAC modules controlled by a Dornier CAMAC data-processor. Special development was needed only for the software.

GENERAL

The installation of crash recorders in commercial aircraft is mandatory and is becoming increasingly common in military aircraft. They enable the cause and history of an accident to be analyzed, by recording a varying number of flight data depending on the aircraft type, on a storage medium which must primarily meet the following requirements:

Indestructibility

The stored data must not be destroyed by the mechanical and thermal stresses occurring during a crash.

Locatability

The data store must be easily locatable after an accident over either land or water.

Recording Length

The store must always contain the latest data recorded immediately before the accident.

These basic requirements have so far given rise to two different types of crash recorder, both of them with the same storage medium consisting of an endless-loop magnetic tape for digital recording.

Armoured Crash Recorder

The tape recorder is encased in a thermal insulating layer and steel or titanium armour and installed in the aircraft rear. This principle has proved acceptable for large, relatively slow aircraft operating solely over land.

Deployable Crash Recorder

An extremely small, light-weight tape recorder is installed in an airfoil whose aerodynamic design is such that it can largely dissipate its kinetic energy before reaching the ground. A built-in radio beacon simplifies location. Its buoyancy enables it to be recovered after accidents over water, unlike the armoured crash recorder. In view of the Alpha Jet's operational profile, a deployable crash recorder was chosen for this aircraft.

For this method of data recovery, the survival probability may be taken to be above 90%.

The recording duration has been fixed at 15 minutes (endless loop). Since the Alpha Jet prototypes contain a telemetry system (SAMUEL), there was no need for a separate data acquisition unit for crash analysis signals. On the other hand an unusually high data rate for a crash recorder (10 kbit per sec compared with, for example, 0.53 kbit per sec for the F-104G) had to be accepted. The crash recorder's electronic system was therefore required to convert the SAMUEL signals, namely:
Channel 1: PCM-NRZ data 2000 bits per sec
Channel 2: PAM-NRZ data 500 words per sec
Channel 3: PAM-NRZ data 500 words per sec

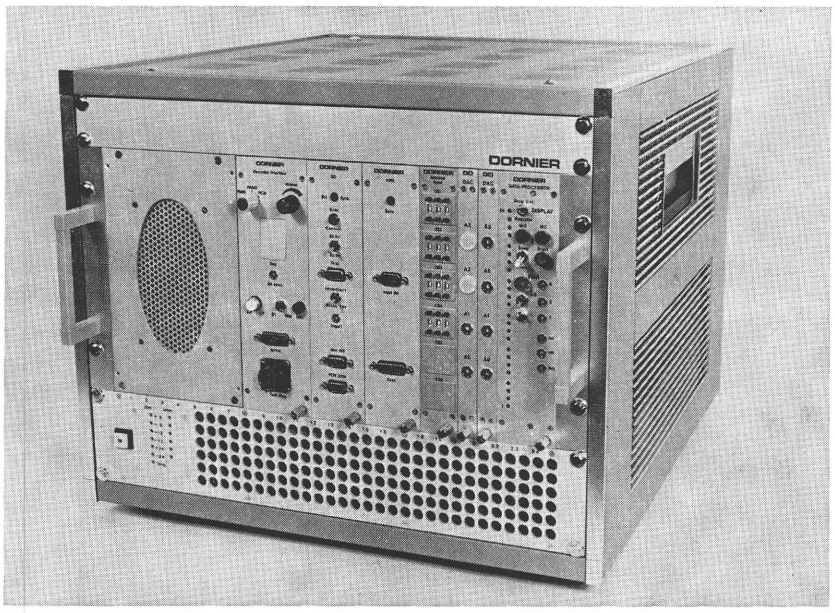

Fig. 1 Alpha Jet Crash Recorder Ground Reproducer Equipment with Dornier CAMAC Modules

into PCM signals for recording by the tape recorder and to record them, together with the aircraft's radio communications traffic.

The interface unit between the SAMUEL telemetry system and the crash recorder in the airfoil is the signal adaption unit. Its job is to convert the three SAMUEL data signals into biphase PCM signals (PCM = pulse code modulation) and to prepare them, along with the cockpit voice signal, for recording on the recorder's four tracks. The recording of the PAM signals (PAM = pulse amplitude modulation) by the PCM technique enables measuring accuracy to be maintained considerably more simply and reliably than by direct PAM recording.

GROUND STATION

The ground station (Figs. 1 and 2) is used for a quick look at the recorder data after a flight or an accident. It provides for:

- reading and decoding of a selectable data track;
- readout of the original PAM formats of of the PCM signal (NRZ);
- readout of four freely-selectable analog channels from the PAM formats;
- play-back of voice.

Provision must be made here for operation independently of the mains power supply.

The part designed for data processing consists for the most part of standard modules from Dornier's CAMAC range. The special recorder interface module amplifies the recorder output signals and adapts them to the CAMAC system. For data reading the recorder can be connected to the ground equipment in two different ways:

- The airfoil is removed from the aircraft and connected to the recorder interface. The power required to operate the recorder is supplied by the ground station.
- The ground station is connected to the test connector in the Alpha Jet's tail via a test cable. This switches on the power module in the signal adaption unit and at the same time prevents new data from being played on to the tape. A test key on the recorder interface enables recording to be switched on again before the Alpha Jet takes off and thus a tape check to be made to test the signal adaption unit.

Reading and decoding of the tape data take place in the bit and frame synchronizer outside the CAMAC bus. The decoded data words from the frame synchronizer are passed via the CAMAC bus to the DAC (one channel), to whose output the complete PAM data frame is connected. In parallel, the four channels, whose addresses are set the channel selector, are read out via the four-channel DAC. The control unit for these processes is the data processor. The program for the above-mentioned command process is stored in a replaceable ROM (read only memory).

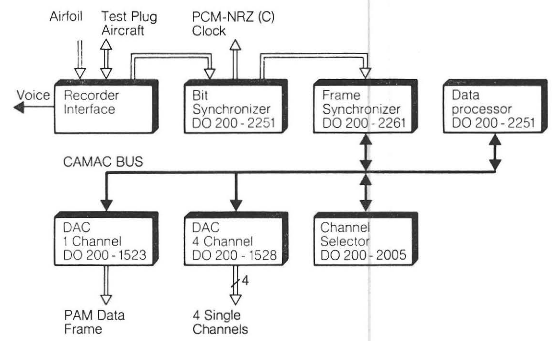

Fig. 2 Block Diagram of Alpha Jet Crash Recorder Ground Reproducer Equipment with Dornier CAMAC Modules.

For operation independently of the mains power supply, the ground station is equipped with two 12V 105Ah truck batteries which automatically supply the CAMAC crate with a.c. power via an inverter when the ground station is not connected to the mains. For operation on the mains the inverter is automatically switched off and the batteries connected to the built-in charging unit.

The complete ground station is installed in a mobile 19-inch cabinet 50cm in height.

NEWS

UNITED KINGDOM CAMAC ASSOCIATION

This Association was officially founded at a meeting of Users and Suppliers of CAMAC equipment in the UK, on 19th June, 1974 at the Middlesex Hospital Medical School, London.

The purpose of the Association is to further the use of CAMAC in the United Kingdom, to represent the interests of a wide cross-section of Users and Suppliers of CAMAC and aid communication between CAMAC Users, Suppliers and bodies administering the CAMAC standards. It will include amongst its principal activities both seminars and exhibitions and will act in coordination with the European CAMAC Association.

At its inaugural meeting the following officers were appointed:

Chairman: Mr. A.C. Peatfield, SRC Daresbury
Vice-Chairman: Mr. D.M. Drury, GEC-Elliott Process Automation Ltd.

The Secretary is Mr. R. North, St. Bartholomew's Hospital, London from whom further details and information can be obtained.

All those in the UK with CAMAC interests are urged to apply for membership which is currently free of charge.

DEVELOPMENT ACTIVITIES

1

CAMAC MODULES FOR ANGULAR SHAFT-POSITION MEASUREMENT

by
F. A. Joerger* and D. W. Zobrist**
* Joerger Enterprises, Westbury, N.Y., USA
** Aluminium Company of America, Pittsburg, PS, USA
Received 23rd July 1974

SUMMARY Versatile CAMAC modules have been designed for obtaining position measurements of rotating shafts. Both angular position and the number of revolutions are calculated and made available to the Dataway. Each module provides in a single unit all that is needed to couple the transducer to the Dataway.

INTRODUCTION

Angular shaft-position signals are often used in industry to measure mechanical rotation or linear displacement. Two types of transducers most often used are shaft-position encoders and synchro transmitters. The position encoders, either optical or brush, are generally used where the shaft-position to be measured is nearby and is in a reasonably friendly environment. Synchro transmitters are normally used when the measured shaft is located some distance from the instrumentation equipment and long wire runs are involved. Synchro transmitters are also used when the transducer must be located in an area of high temperature, vibration, or other hostile environment. When absolute-angle information is not required, dual-phase incremental encoders may be used.

Three CAMAC modules (Fig. 1) have been designed to provide the necessary instrumentation to receive signals from such transducers and process them for the system. Each module/transducer combination is interchangeable with the others. To the Dataway they look identical. This simplifies the software requirements and enhances the flexibility of the units. For example, an optical shaft-encoder and shaft-encoder receiver module can readily be replaced with a synchro-transmitter and synchro-receiver module for remote operation. No other hardware and no software changes are required.

SIGNAL PROCESSING

The synchro-receiver module accepts three-wire stator signals and two-wire rotor reference signals from a synchronous transducer (synchro). Conventional Synchro-to-Digital signal processing is done, along with electronic turns-counting for extended range operation. (This eliminates considerable software overhead that might otherwise be required).

The shaft-encoder receiver module accepts gray-coded binary signals from optical or brush encoders. The module provides the necessary signal-line receivers, gray to straight-binary conversion, data buffering, and turns-counting logic.

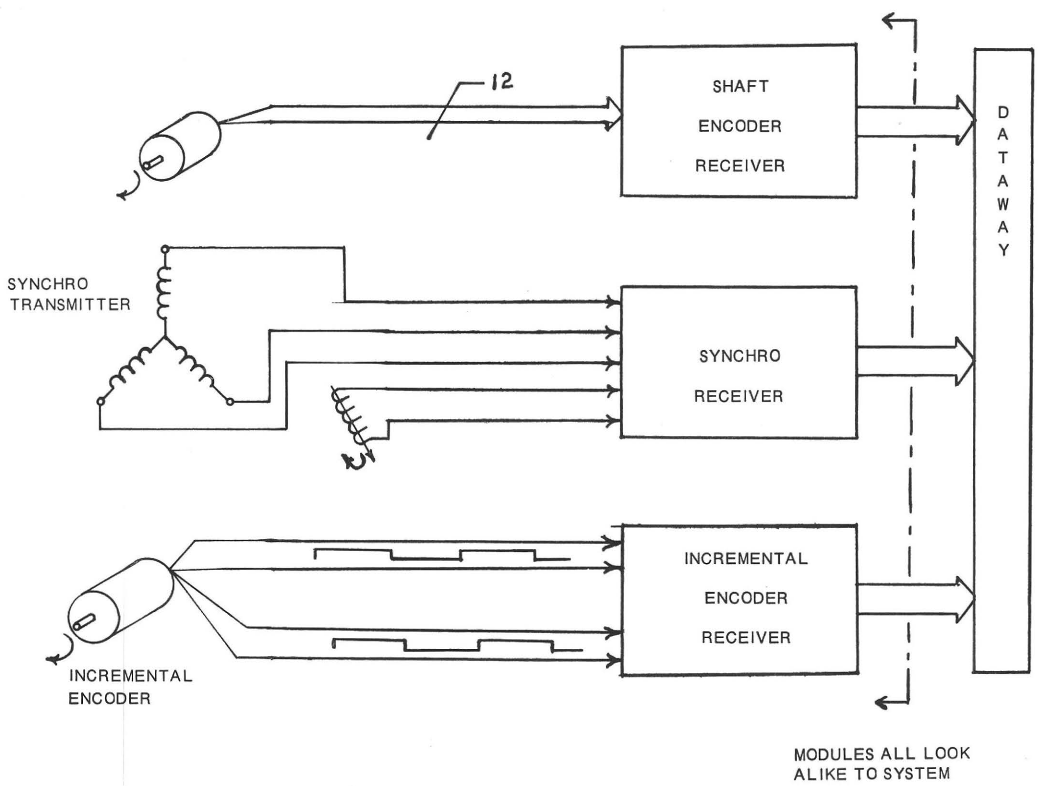

Fig. 1 Transducer/Module Combinations for Angular Shaft Position Measurements

The incremental-encoder receiver accepts dual-phase pulses (90 degrees apart) from the transducer. The module determines the direction of shaft movement and counts the number of increments moved.

CAMAC COMMANDS

The angular data is read with an N.F(0).A(0) command and the turns-count information with an N.F(0).A(1) command. Data which is not absolute, such as the turns-count, may be overwritten with an N.F(16) command. In all modules, both the angular data and the turns-count are presented to the Dataway right-justified with sign extension. That is, the most significant bit is repeated on all the upper Dataway read lines. This provides software compatibility regardless of the computer word size.

CONCLUSION

The CAMAC standard has been successfully applied to functional instrumentation for angular position signals. These units are extremely useful, as they require less software overhead (and no additional conditioning hardware).

CAMAC CORRESPONDENCE

Charles E. Cohen, Argonne National Laboratory, has commented on the article 'SHIFT — a Serial Highway Interface for Teletypes' by Douglas L. Abbott, Jülich Laboratory, who has replied. Reference *CAMAC Bulletin* Issue No. 10, July 1974.

COHEN

Two points need to be made with respect to arrangements of this type. First, is it really logical to use a teletype port to interface the computer to the adaptor? It is wasteful of hardware to convert data from parallel to serial in the teletype port and then reconvert it to parallel in the adaptor for further processing. Consequently, in Figure 1 of the paper, the upper left-hand terminal receiver and the lower right-hand terminal transmitter should be omitted and communication with the computer be via a parallel interface.

ABBOTT

Perhaps I did not make clear in the article that some people really want to use the teletype port from their computer as a connection to the Serial Highway. In fact, many of the design parameters of the Serial Highway were chosen to make this type of connection practical. This is particularly useful for users with little experience in computer interfacing and/or system software. The connection usually requires no more than four wires and the existing system I/O handlers for the teletype can drive the Serial Highway with little or no modification.

Certainly as you suggest, the upper left-hand terminal receiver and the lower right-hand terminal transmitter could be replaced by parallel interfaces to the computer. But this defeats the purpose of the module, which is to simplify the computer connection by taking advantage of the most widely recognised and used computer interfacing standard—the teletype port. And besides, hardware is cheap compared with the cost of getting a system up and running.

The extra serial-parallel and parallel-serial conversions are only necessary for automatic delimiter generating and stripping. If one were content to handle that in software, then SHIFT reduces to little more than a bit-by-bit synchronizer.

COHEN

Secondly it is possible, under some circumstances, that the computer could not keep up with the stream of data coming down the highway. The adaptor as shown contains no provision to prevent data from being lost in that instance. What is needed is an arrangement to inhibit the automatic generation of delimiter bytes, holding the dataway in the pause state, whenever an input byte is waiting to be read by the computer. Analogous deferral of the generation of non-delimiter bytes is a programming function.

ABBOTT

Your second point is well taken. We had reached the same conclusion but only after the paper was accepted for publication. Our solution was to make delimiter generation and stripping a programmable option thereby making the program responsible for deciding when it is unable to accept messages. Your solution appears cleaner and we will certainly consider incorporating it in our next design. The programmable option may still be useful for other reasons.

I should perhaps also point out that it was not the intention of the article to say that this is how one *should* interface to the Serial Highway. Clearly, if the data rate exceeds maybe 50-100 kHz a more sophisticated driver (both in hardware and software) is necessary. But I think it does show that, when system parameters permit, it is possible to take advantage of the inherent simplicity of the standard teletype port.

2

A CAMAC BRANCH DRIVER FOR THE PDP-8/E COMPUTER

by

M. Nadachowski* and J. Bundgaard

Research Establishment, Risø, Denmark
* On leave from Institute of Nuclear Research, Swierk, Poland

Received 8th October 1974

SUMMARY This relatively simple branch driver connects a CAMAC Branch Highway to a PDP-8/E computer. The driver occupies three DEC mounting boards, which are inserted directly into the OMNIBUS of the computer.

GENERAL

A CAMAC branch driver for the PDP-8/E computer, compatible with the EUR4600e specification has been developed at the Research Establishment Risø. It is used, in conjunction with an existing computer, for testing CAMAC equipment. The driver enables either programmed transfers or program interrupt transfers of information between the computer and a CAMAC branch. The block diagram in Fig. 1 shows the main parts of the device.

The 12-bit MSB and LSB data registers are accessible from the computer OMNIBUS as well as from the CAMAC branch highway. Their contents may be encoded in a 23-input priority encoder, which speeds up demand handling.

A 12-bit ACN address register is loaded with subaddress, crate number and station number before every CAMAC. The accumulator is cleared when its contents are loaded into any of the driver registers.

Q, X and interrupt enable flip-flops are included in the driver, but there is no device flag, because the BD line is used directly as the flag signal.

The driver contains branch terminating pull-up resistors.

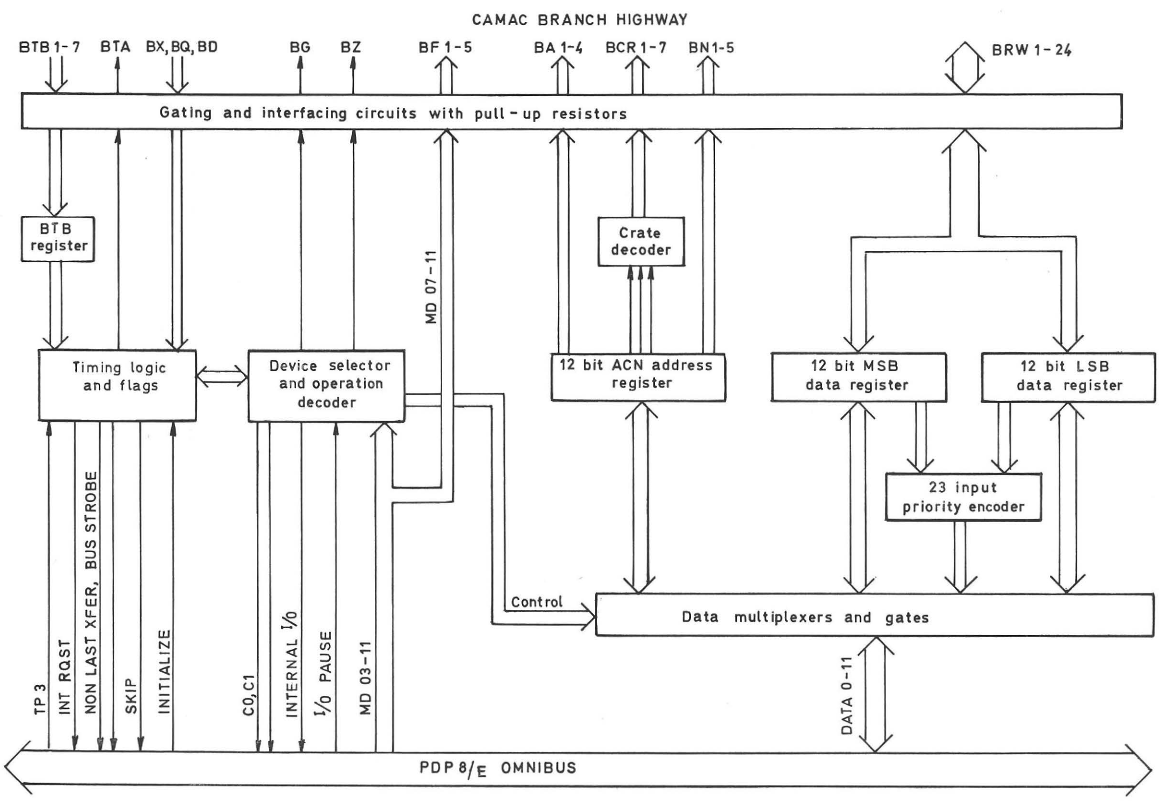

Fig. 1 Block Diagram of the Branch Driver

INSTRUCTIONS IMPLEMENTED

The driver uses 6 of 64 possible PDP-8/E peripheral device addresses. Four PDP-8 device addresses are used to generate 32 CAMAC functions as shown in Fig. 2. The F1 to F16 bits are transferred directly to the branch highway. Only the F16 and F8 bits are tested in the driver to produce BRW gating signals.

Two other PDP-8 device addresses are occupied to generate 16 commands used by the driver: 14 non-CAMAC instructions and 2 special CAMAC instructions. The non-CAMAC instructions include:

- bidirectional exchange of data between the accumulator and MSB, LSB, and ACN registers;
- testing Q, X, BD and error flags;
- enabling and disabling interrupts in the driver;
- saving and restoring Q and X, which are useful for powerfail handling;
- reading the encoded contents of the MSB and LSB registers.

Two special CAMAC instructions generate the Branch Initialise BZ signal and the Graded-L Request BG signal.

a)

MD	0	1	2	3	4	5	6	7	8	9	10	11
a)	1	1	0	X	X	X	Y	F16	F8	F4	F2	F1
	I/O operation code			Selectable code				CAMAC function code				

b)

MD	0	1	2	3	4	5	6	7	8	9	10	11
b)	1	1	0	X	X	X	$\bar{Y}$	Z	I_8	I_4	I_2	I_1
	I/O operation code			Selectable code					Command code			

Fig. 2 IOT Instruction Format: a) CAMAC Instructions, b) Non CAMAC Instructions and 2 special CAMAC Instructions implemented by the Driver

TIMING

Computer timing is stopped during the execution of CAMAC instructions. The CAMAC commands generate a NOT LAST XFER signal which halts the computer timing until the CAMAC cycle is completed. The execution time of CAMAC operations is approximately 2.5 μs depending on the Type A controller used. The driver has a time-out control system which restarts the computer if a CAMAC instruction does not produce a response (BTB signals) within 1 ms. Upon restart an error flag is set.

CRATE ADDRESSING

There are two possibilities of crate addressing in the driver: either only one crate or all on-line crates may be addressed at the same time. Addressing all on-line crates takes place during Graded-L Request, but may also be brought about by issuing the crate address CR = 0.

DEMAND HANDLING

The Branch Demand may be checked in a computer program by means of the SKIP ON BD instruction, or it may cause a program interrupt if that facility is enabled in the driver and in the computer. The method used for determining the source of L request depends on the LAM sorting hardware in the crates.

In the simplest case the crates are not equipped with special LAM-Grader units. LAM Graders are replaced by simple wiring on the rear connectors of the crate controllers. In this case the commands CR(j) N(30) A(0) F(0) are used to read the GL words of crates in a sequence selected by the program (for example j = 1, 2..., 7). In this way the GL patterns of addressed crates are successively loaded into the MSB and LSB registers in the driver. The crate search is continued until the first crate giving a non-zero GL-word is found. The highest priority LAM-source in that crate, encoded in the priority encoder, is used, in conjunction with the crate number, to find the appropriate service routine in the program.

The LAM-search procedure described above is long and time consuming. It may be simplified by using LAM-grader units for fast identification of crates with active L requests. In a LAM Grader module based on the ideas suggested in Ref. 1, each of the last 7 bits of the GL-word is used as the combined ORed LAM signal from all the modules in that crate. The last 7 bits of the GL-word thus give the identity of crates that are sending demands. The LAM-Grader module should also permit its LAM pattern word to be read by A(o) F(o) addressed to the station number of the LAM-Grader module. In a branch equipped with such a LAM-Grader unit, the LAM source search is limited to the following steps:

- reading the identity of crates sending demands by Graded-L Request (BG);
- encoding the number CR(R) of the highest priority crate with an active L request, using the priority encoder in the driver;
- reading the LAM pattern of that crate by means of CR(R) N(i) A(o) F(o), where (i) is the station number of the LAM-Grader unit;
- encoding the highest priority LAM source module N(m), using the priority encoder;
- finding the proper service routine for module m in crate R.

The 17 free bits in the GL-word may be used for privileged demand sources.

EXAMPLES OF PROGRAMMING

Program examples for bidirectional transfer of 24-bit CAMAC words between the memory of the computer and a register in a CAMAC module are shown below.

Write a 24-bit CAMAC word

```
      ,
      ,
      ,
TAD ACN / Get module address
WACN    / Load ACN register
TAD LSB / Get 12 less-significant bits of data
WLSB    / Load LSB register
TAD MSB / Get 12 most-significant bits of data
WMSB    / Load MSB register
SF16    / Send CAMAC function F(16)
      , / Write data to a module
      ,
      ,
```

Read a 24-bit CAMAC word

```
      ,
      ,
      ,
TAD ACN / Get module address
WACN    / Load ACN register
SFO     / Send F(o) to read a CAMAC word
          to the MSB and LSB registers
RLSB    / Read LSB register to accumulator
DCA LSB / Store LSB in memory
RMSB    / Read MSB register to accumulator
DCA MSB / Store MSB in memory
      ,
      ,
      ,
```

REFERENCE

1. Trebst, H.-J., Methods of Demand Handling; *CAMAC Bulletin*, No. 4, July 1972, p. 3.

3

A CAMAC SERIAL DRIVER-RECEIVER

by

G. Messing*, J. Stolte and E. Kwakkel

Institute for Nuclear Physics Research, Amsterdam, The Netherlands
*Central Research Institute for Physics, Budapest, Hungary

Received 25th October 1974

SUMMARY A serial driver-receiver has been developed for controlling remote experiments. The driver-receiver controls a CAMAC Serial Highway loop and contains an interface for the ALPHA-16-LSI-2 mini-computer. The devices connected to the serial loop are adapters to parallel Branch Highways.

INTRODUCTION

To control experimental equipment distributed over a large area the CAMAC Serial Highway System[1] successfully combines the convenient features of the widely-used CAMAC system and the economy of a serial data transfer system. A Serial Driver-Receiver (SDR) has been designed to act as an interface between the computer, in this case an ALPHA 16-LSI-2, and the serial CAMAC loop. The devices connected to the Serial Highway need not be Serial Crate Controllers, and in this particular case they are Serial Branch Adapters[2] (SBA), which interface the serial loop to standard CAMAC Branch Highways. The terminology used in this paper differs from that in Ref. 1, and follows an early unpublished document on the Serial Highway.

MESSAGE FORMATS

Messages sent by the SDR contain four or eight bytes, followed an appropriate number of consecutive idle bytes (three bytes in a Write or Control Message, seven in a Read Message) which will be replaced by the Reply Message from the addressed SBA. When no message is generated, the SDR continuously sends zero bytes along the serial loop, to enable the SBA's to switch out their possibly filled 4-byte delay and to send Demand Messages (if LAM flags are pending). Though bytes sent by the SDR or by the SBA's always have one stop bit, the SDR is able to handle bytes with an unlimited number of stop bits.

To generate a serial message, the necessary information (CR, N, A, F, W) must first of all be buffered in the SDR. Received serial Reply and Demand Messages are also buffered in the SDR. Information is exchanged between the computer and SDR by normal computer input-output instructions. Computer message-formats are shown in Fig. 1.

OPERATION

The block diagram of the SDR is shown in Fig. 2. The Computer Interface contains hardware to execute input-output computer instructions, to set interrupts and interrupt restart addresses, etc.

Before a message is generated, the initial information (CR, N, A, F, W) must be transferred to the Sender Register. When all these data have been buffered, the Sender Timing starts to send the

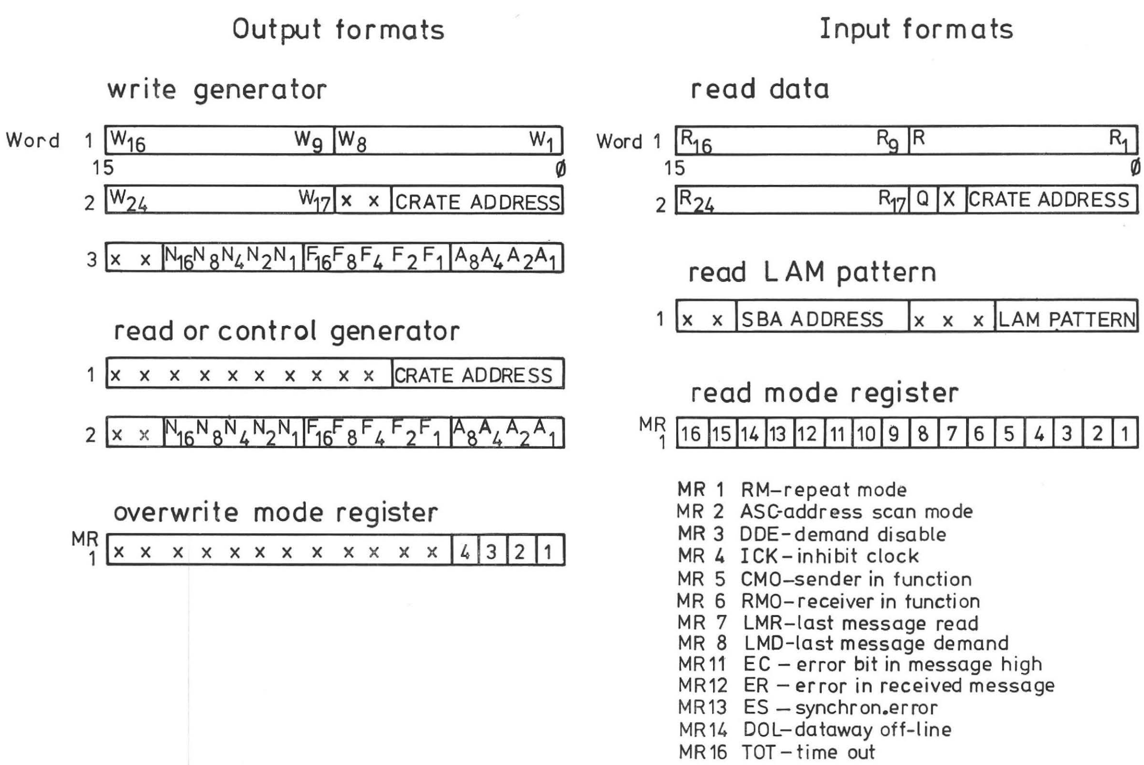

Fig. 1 Computer Message Formats

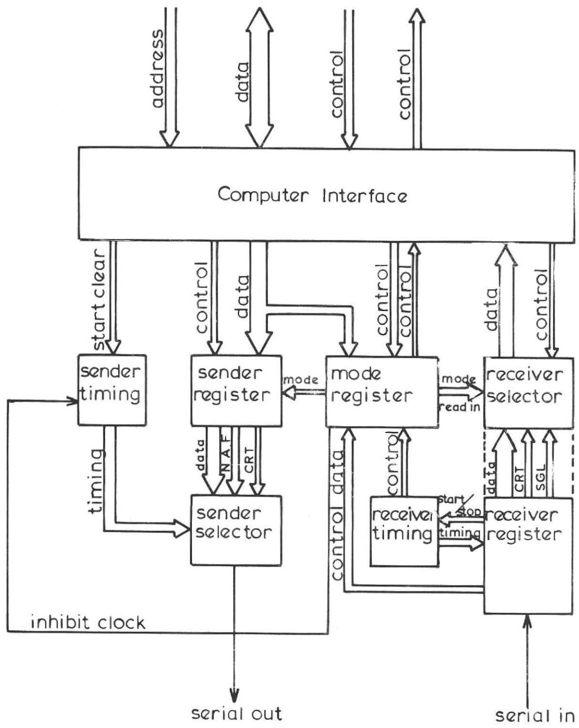

Fig. 2 Block Diagram of the Serial Driver-Receiver

Command Message via the Sender Selector. The Sender Selector contains the sender shift register into which the message is written byte-by-byte from the Sender Register and clocked out bit-by-bit according to the preselected clock frequency. Received bit-serial information will be clocked into the receiver shift register. A routine in the Receiver Timing continuously looks for zero bytes in the incoming information.

When a zero byte arrives, the receiver timing regards the next incoming byte (if not a zero byte) as the header-byte of a message and starts to store the information byte-by-byte in the Receiver Register. If the message is a Read or Demand Message, or a message error has been detected, the sender clock (the only clock in the serial loop) will be inhibited and an interrupt request will be generated. After receipt of the interrupt-acknowledge signal the SDR sets one of the three possible restart addresses according to the interrupt source: read data, demand or error.

The SDR Mode Register (for bit configuration see Fig. 1) contains up-to-date information about the mode of operation and status of the SDR. The Mode Register can be read by the computer at any time and can be partly overwritten. Four bits can be defined by the computer: Repeat Mode, Address Scan Mode, Demand Disable and Inhibit Clock. When the Repeat Mode flip-flop is set, the Sender Timing starts to repeat the message sent previously after having received an error-free Reply Message.

When the Address Scan flip-flop is set, the SDR increases the subaddress pattern by 1 and, after having received the Reply Message, starts to send the otherwise unchanged message. If the subaddress register overflows, it will be set to zero and the contents of the N register will be increased by one.

The Mode Register contains three error flip-flops indicating whether an error has been detected in the Command Message received by the SBA (EC), whether an error has been found in the Reply- or Demand Message received by the SDR (ER), or a synchronisation error (ES) has occurred. The TOT bit will be set when, within a specified time, no Reply Message has been received to answer a Command Message. The bits LMD and LMR indicate whether the last received message has been a demand or read-reply. The bits CMO and RMO indicate whether the SDR sender is actually sending or the SDR receiver is receiving a message.

The SDR has been built in a modular way. Interfacing to other 16 or 8 bit computers will not be complicated.

REFERENCES

1. CAMAC Serial System Organization — A Description. U.S.AEC NIM Committee, TID 26488; ESONE Committee, ESONE/SH/01, Dec. 1973.
2. Kwakkel, E., Messing, C., A CAMAC Serial Branch Adapter, *CAMAC Bulletin*, No. 9, March 1974, p. 15.

NEWS

U.S. CAMAC INDUSTRIAL APPLICATIONS GROUP (CIAG)

This recently formed Group has been set up to encourage and enable an informal "off-the-record" exchange of ideas and information regarding the use of CAMAC in industrial applications. Its first meeting, August 6th 1974, was attended by 16 people from 11 organizations and the second meeting, October 7th 1974, by 35 people from 25 organizations.

This second meeting was characterized by contributions from ALCOA, NASA-LEWIS and Lawrence Livermore Laboratory on their CAMAC applications and a discussion of "Grounding and Shielding" practices. The summary of this discussion is available on request from the Chairman, D.W. Zobrist, ALCOA, Pittsburgh. A study group was set up to look into recommendations for grounding practices.

The CIAG had its third meeting on February 4th 1975 at the Louisiana State University, one day before the Tenth Annual Conference on the use of Digital Computers in Process Control at the same place (February 5-7, 1975). Beside other events a discussion of the 23-crate CAMAC serial Highway installation at ALCOA for furnace control has taken place and a digital control demonstration using CAMAC was set up.

Everyone interested in applying CAMAC to industrial applications is invited to join the CIAG. Although the CIAG is a CAMAC User's Group, endors are invited to attend and take part in the meetings to acquaint themselves with the needs of end-users.

ESONE-NIM COMMITTEES
ACTIVITIES OF THE CAMAC WORKING GROUPS

The ESONE Committee in Europe and the U.S.AEC NIM Committee in America have both authorised different working groups to investigate specific aspects of CAMAC. The European and American working parties are performing their activities in close collaboration.

ESONE-CAMAC WORKING GROUPS

Dataway Working Group

Chairman: R. Patzelt, TH, Wien

The second set of amendments and errata to the Description of the Serial Highway has been finished and will be published. The most important change, confirming a preliminary announcement, is the definition of new signal specifications conforming to standards developed by ISO and EIA. The new standard gives improved performance and allows easy handling by i.c.-elements. Additionally, some unnecessary restrictions in the message-handling are withdrawn, so that now multi-crate operations are, in principle, possible. Other items are under consideration, not to change the SH-Specification but to provide extensions that cover multi-crate operations, block-transfers, the minimum specifications for compatible message formats and recommendations for serial drivers. Slight improvements in the solution of the difficult compromises between safety and efficiency with respect to byte and message synchronisation are also under current discussion.

The text of the final specification could benefit from operational experience with early (Serial Highway) systems. The difficult problem of standardising an alternative to the 'Stop' mode of block transfers was discussed further. It seems to be nearly impossible to find a solution but makes the new mode available for applications, where it is appropriate, without appearing to weaken the status of the existing 'Stop' mode. In an attempt to meet conflicting demands in ESONE and NIM, the Working Group prepared a new presentation of its previously agreed proposal.

Software Working Group

Chairman: I.N. Hooton, AERE, Harwell

'The Definition of IML (A Language for Use in CAMAC Systems)' has now been published as an ESONE Secretariat Document ESONE/IML/01 and in the USA as TID 26615. Any comments should be sent to members of the appropriate Software Working Group. It is hoped to produce a model User's Guide which can be adapted to a specific implementation. Syntactic versions of IML to suit higher language environments are to be considered, starting with BASIC.

Simple additions to BASIC for module testing are already under consideration and a recommendation is expected shortly.

Information Working Group

Chairman: H. Meyer, CBNM-CRC, Euratom, Geel, Belgium

At its last meeting, the Working Group decided upon several changes to the CAMAC Bulletin in order to reinforce the promotional effort on CAMAC applications:

— Information which is of primary interest to member institutes and associated laboratories of the ESONE/NIM Committees will be put together in a separate section of the CAMAC Bulletin. This will underline the fact that CAMAC is not just of interest to the ESONE/NIM laboratories but is useful for applications elsewhere.

— A Readers Service Enquiry Card, as published for the first time in this issue, should assist the collection by readers of information on CAMAC products and systems. Enquiry Cards which are returned to the given address will be sent to the companies concerned for their response.

— More tutorial presentations on CAMAC and its use will be initiated.

In addition the Information Working Group will be arranging the translation into different languages of the more interesting papers and reports that appear from time to time so that the promotional value of these will be enhanced and not impeded by language problems. For instance, a translated paper could be offered for publication in a periodical whose readership would not be able to read the paper in its original language.

NIM-CAMAC WORKING GROUPS

NIM Committee

Chairman: L. Costrell, National Bureau of Standards, Washington

The US NIM Committee and its working groups met in conjunction with the 1974 Nuclear Science Symposium in Washington, D.C. in December. R.C.M. Barnes of Harwell, K.D. Müller of KFA Jülich and Ph. Ponting of CERN participated in the meetings. The NIM-Industry Luncheon, arranged annually for informal discussions between manufacturers and NIM Committee members, was also held at that time. The Dataway and Software Working Groups are scheduled to meet next in the week of March 24th at Florida State University in Tallahassee.

Dataway Working Group

Chairman: F.A. Kirsten, Lawrence Berkeley Laboratory

The NIM Dataway Working Group (NDWG) has continued to concentrate its efforts on the Serial Highway System. Since the description was jointly issued by NIM and ESONE in December 1973 and as Serial System components have been built and put into service, the need for certain additions and revisions have become apparent. NDWG and its ESONE counterpart have prepared and issued Addendum and Errata to the Description.

The Description contains a request that designers

of Serial System components maintain close touch with the working groups. The NDWG is particularly appreciative of the efforts of Kinetics Systems Corporation and Jorway Corporation in this regard.
Their cooperation in maintaining this communication has been very important in the work on the revision.

A second important topic has been Block Transfers. In joint meetings with the NIM Software Working Group, this has received careful attention. Those attending the Washington meeting were optimistic that some significant progress had been made.

The relation of CAMAC to other data structures and standards is being followed by the Compatibility Sub-group. A standard of importance in this regard, the Electronic Industries Association definition of a balanced signal standard for binary-data interchange, has been adopted for the 'D'-ports of the Serial Highway.

Software Working Group

Chairman: R.F. Thomas Jr., Los Alamos Scientific Laboratory

The NIM Software Working Group, at its meeting December 11th in Washington, reviewed and responded to a list of errata and addenda to the IML document. Further consideration was given, in a joint meeting with the Dataway Working Group, to the problem of preferred modes of block transfer in CAMAC. The Working Group considered for the first time a draft of a proposed CAMAC Software Handbook. Extensive modifications and additions to this document were agreed, in principle, and a new draft should be ready for the March meeting.

NEWS

NIM INDUSTRY LUNCHEON MEETING

This annual event brings together the NIM Committee and the major users and manufacturers. After a lunch (noted for its high price and uninteresting menu) there is a review of the current status of the NIM and CAMAC standards.

This year's meeting, 10th December 1974 in Washington, was the 10th anniversary of the formation of the NIM Committee and the first publication of the NIM standard. The NIM system is still flourishing, and has integrated sales of perhaps $100M to its credit. But it is now so stable that discussion at the meeting was almost entirely about CAMAC, apart from some nostalgic references to the early days of NIM.

After reports by the Chairmen of the NIM-CAMAC Working Groups (see elsewhere in this issue) there were impressive statements from some major users of CAMAC. For example, Dale Zobrist of ALCOA mentioned the 23-crate system, now on order, to control 46 furnaces. This system uses the CAMAC Serial Highway in bit-serial mode at the maximum clock rate of 5 MHz. The clock and data are multiplexed onto the same coaxial cable, and there is switching between the main serial loop and a reserve loop to improve system security. ALCOA find CAMAC attractive because it is an established standard, with second-sourcing of equipment, and with at least six US computer firms willing to supply their computers with CAMAC interfaces.

Describing the use of CAMAC at the Fermi National Accelerator Laboratory, Gordon Kerns said they have 26 multi-crate CAMAC systems with PDP-11 computers, and have ordered 20 Serial Crate Controllers for use in the experimental areas. CAMAC is also used in a network, with cable lengths up to 10 000ft (3km), interconnecting the PDP-11's to a CDC 6600.

The report from the CAMAC Industry Applications Group again showed the tendency to distinguish between 'CAMAC equipment' conforming fully to the specifications and 'CAMAC-compatible' equipment that does not necessarily conform fully but can nevertheless be used in conjunction with, and without restricting the performance of, 'CAMAC equipment'.

ESONE CHAIRMAN 1974/75

Owing to the recent, lamentable death of Mr. Brian Macefield of Oxford University, who was elected ESONE Chairman at the Annual General Assembly in Warsaw, a new Chairman has been elected. He is Mr. Fred Iselin of the CERN Laboratory, 1211 Geneva 23, Switzerland, Tel (022) 41 98 11, Telex: 23698.

CAMAC PRODUCT GUIDE

AMENDMENTS TO ISSUE 11 (HARDWARE)

This guide consists of a list of CAMAC equipment which is believed to be offered for sale by manufacturers in Europe and the USA. The information has been compiled by CERN–NP–Electronics and is mainly based on information communicated by manufacturers and available up to the 31st January 1975.

Every effort has been made to ensure the completeness and accuracy of the list, and it is hoped that most products and manufacturers have been included. Inclusion in this list does not necessarily indicate that products are fully compatible with the CAMAC specifications nor that they are recommended or approved by the ESONE Committee. Similarly, omission from this list does not indicate disapproval by the ESONE Committee.

Reader service starts this issue. You are advised to use the reader service card, inserted in this Bulletin, if you wish to obtain more information on CAMAC Products, and to be on manufacturers mailing lists for current information on their products.

Entries are grouped in new –N–, corrected –C–, and deleted –D– products, and each is arranged according to product class.

A full listing of products was published in No. 11 and will appear again in No. 13 of the Bulletin.

Remarks on some columns in the Index of Products

Column

NC – N is new, C is corrected entry.

CODE – Classification code, a 2- or 3-digit decimal number (see below).

WIDTH – 1 to 25, indicates module width or—for crates—the number of stations available.
– 0 indicates unknown width or format.
– Blank, the width has no meaning.
– NA indicates other format, normally a 19 inch rack mounted chassis.

NPR – Number in brackets is issue number of the Bulletin in which the item was or is described in the New Products section.

DELIV – Date on which item became or will become available.

CLASSIFICATION GROUPS

code

1 **DATA MODULES** (I/O Transfers and Processing)

11 **Digital Serial Input Modules** (Scalers, Time Interval and Bi-directional Counters, Serial Coded etc.) . . . .

12 **Digital Parallel Input Modules** (Storing and Non-Storing Registers, Coinc. Latch, LAM, Status etc.) . . . .

13 **Digital Output Modules** (Serial: Clocks, Timers, Pulse Generators, Parallel: TTL Output, Drivers) . . . .

14 **Digital I/O, Peripheral and Instrumentation Interfacing Modules** (Serial and Parallel I/O Regs, Printer-, Tape-, DVM-, Plotter- and Analyser Interfaces, Step-Motor Drivers, Supply CTR, Displays) . . . . . .

15 **Digital Handling and Processing Modules** (and/or/not Gates, Fan-Outs, Digital Level and Code Converters, Buffers, Delays, Arithm. Processors etc.) . . . .

16 **Analogue Modules** (ADC, DAC, Multiplexers, Amplifiers, Linear Gates, Discriminators etc.) . . . .

17 **Other Digital and/or Analogue Modules** (Mixed Analogue and Digital, Not Dataway Connected etc.) . . . .

2 **SYSTEM CONTROL** (Computer Couplers, Controllers and Related Equipment)

21 **Interfaces/Drivers and Controllers** (Parallel Mode for 4600 Branch and Other Multi-Crate Bus, Single-Crate Systems, Autonomous Systems) . . . .

22 **Interfaces/Controllers/Drivers for Serial Highway** . . . .

23 **Units Related to 4600 Branch or Other Parallel Mode Control/Data Highway** (Crate Controllers, Terminations, LAM Graders, Branch/Bus extenders) . . . .

3 **TEST EQUIPMENT**

31 **System Related Test Gear** . . . .

32 **Branch Related Testers/Controllers and Displays** . . . .

33 **Dataway Related Testers and Displays**

34 **Module Related Test Gear** (Module Extenders) . . . .

37 **Other Test Gear for CAMAC Equipment**

4 **CRATES, SUPPLIES, COMPONENTS, ACCESSORIES**

41 **Crates and Related Components/Accessories** (Crates with/without Dataway and Supply, Blank Crates, Crate Ventilation Gear)

42 **Supplies and Related Components/Accessories** (Single- and Multi-Crate Supplies, Blank Supply Chassis, Control Panels, Supply Ventilation) . . . .

43 **Recommended or Standard Components/Accessories** (Branch Cables, Connectors etc., Dataway Connectors, Boards etc., Blank Modules, Other Stnd Components) . . . .

AMENDMENTS TO
INDEX OF PRODUCTS

NEW ITEMS

NCD	CODE	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	RS. REF.
N	,111	QUAD SCALER (4X24BIT, 300MHZ, 7-SEGMENT DISPLAY/SCALER, OVF GIVES LAM)		SCHLUMBERGER	3		(12)	12,1001
N	,111	DUAL SCALER (2X16BIT, 50MHZ)	DS 050	STND ENGINEERING	1	/73		12,1002
N	,111	DUAL SCALER (2X16BIT, 100MHZ)	DS 100	STND ENGINEERING	1	/73		12,1003
N	,111	DUAL SCALER (2X16BIT, 150MHZ)	DS 150	STND ENGINEERING	1	/74		12,1004
N	,111	DUAL SCALER (2X16BIT, 200MHZ)	DS 200	STND ENGINEERING	1	/74		12,1005
N	,111	QUAD SCALER (4X16BIT, 50MHZ)	QS 050	STND ENGINEERING	1	/73		12,1006
N	,111	QUAD SCALER (4X24BIT OR 2X48BIT,100MHZ, OVF GIVES LAM, COMMON INHIBIT GATE)	QS 100	STND ENGINEERING	1	/73	(12)	12,1007
N	,111	QUAD SCALER (4X16BIT, 150MHZ)	QS 150	STND ENGINEERING	1	/74		12,1008
N	,111	QUAD SCALER (4X16BIT, 200MHZ)	QS 200	STND ENGINEERING	1	/74		12,1009
N	,113	BIN,PRESET SCALER/BCD-DISPLAY(24BIT/8DEC 50MHZ,DATAWAY SET,2I/P&GATE MODES,INHIB)	C-SD-24	WENZEL ELEKTRONIK	1	/75		12,1010
N	,121	INPUT GATE (2X24BIT STATIC DATA,INTEGR FOR 10USEC,TTL LEVELS,2X37-WAY I/P CONN)	321A	POLON	1	/74		12,1011
N	,121	(SAME, INTEGRATION FOR 5MSEC)	321B		1	/74		
N	,121	ISOLATED INPUT GATE(16BIT,VERSION AG302D FOR 12,24 OR 48V, AG302A FOR 115VAC)	AG 302*	STND ENGINEERING	1	/74		12,1012
N	,121	INPUT GATE (16BIT, CONTACT CLOSURE)	AG 302C	STND ENGINEERING	1	/74		12,1013
N	,121	INPUT GATE (16BIT)	PG 301	STND ENGINEERING	1	/73		12,1014
N	,121	INPUT GATE (24BIT)	PG 304	STND ENGINEERING	1	/73		12,1015
N	,121	DUAL INPUT GATE (16BIT)	PG 601	STND ENGINEERING	1	/73		12,1016
N	,122	ISOLATED INPUT REGISTER(16BIT,AR302D FOR 12,24 OR 48VDC, AR302A FOR 115VAC)	AR 302*	STND ENGINEERING	1	/74		12,1017
N	,122	INPUT REGISTER (16BIT,CONTACT CLOSURE)	AR 302C	STND ENGINEERING	1	/74		12,1018
N	,122	INPUT REGISTER (16BIT)	PR 301	STND ENGINEERING	1	/73		12,1019
N	,122	INPUT REGISTER (24BIT)	PR 304	STND ENGINEERING	1	/73		12,1020
N	,122	DUAL INPUT REGISTER (16BIT)	PR 601	STND ENGINEERING	1	/73		12,1021
N	,122	DUAL INPUT REG,(2X24BIT,SEP,TIMING,LOGIC BITWISE POS/NEG,4TIMING& 3DATA IN MODES)	C-IC-48	WENZEL ELEKTRONIK	1	/75		12,1022
N	,123	16BIT DISCRIMINATOR-COINCIDENCE REGISTER	2352	BI RA SYSTEMS	2	01/75		12,1023
N	,123	COINCIDENCE REGISTER/LATCH (16 CHANNEL)	CR 116	STND ENGINEERING	1	/74		12,1024
N	,123	COINCIDENCE REGISTER/LATCH (16 CHANNEL)	CR 216	STND ENGINEERING	1	/74		12,1025
N	,123	COINCIDENCE REGISTER/LATCH (24 CHANNEL)	CR 224	STND ENGINEERING	1	/74		12,1026
N	,123	COINCIDENCE REGISTER (16 CH,COMMON GATE, MIN OVERLAP 2NS,DOUBLE PULSE RESOL 10NS)	CR-6001	STND ENGINEERING	1	/74	(12)	12,1027
N	,124	MANUAL REGISTER (FOUR 16 BIT WORDS)	231	POLON	3	/74		12,1028
N	,127	ISOLATED INTERRUPT GATE(16BIT,*=D FOR 12,24 OR 48V,*=A FOR 115VAC VERSION)	AIG 302*	STND ENGINEERING	1	/74		12,1029
N	,127	INTERRUPT GATE (16BIT,CONTACT CLOSURE)	AIG 302C	STND ENGINEERING	1	/74		12,1030
N	,127	ISOLATED INTERRUPT REGISTER(16BIT,*=D FOR 12,24 OR 48VDC,*=A FOR 115VAC)	AIR 302*	STND ENGINEERING	1	/74		12,1031
N	,127	INTERRUPT REGISTER(16BIT,COTACT CLOSURE)	AIR 302C	STND ENGINEERING	1	/74		12,1032
N	,127	INTERRUPT GATE (24BIT)	IG 304	STND ENGINEERING	1	/74		12,1033
N	,127	DUAL INTERRUPT GATE (24BIT)	IG 604	STND ENGINEERING	1	/74		12,1034
N	,127	INTERRUPT REGISTER (12BIT)	IR 012	STND ENGINEERING	1	/74		12,1035
N	,127	INTERRUPT REGISTER (16BIT)	IR 016		1	/74		
N	,127	INTERRUPT REGISTER (24BIT)	IR 024		1	/74		
N	,127	INTERRUPT REGISTER (24BIT)	IR 304	STND ENGINEERING	1	/74		12,1036
N	,131	TEST PULSE GENERATOR (NIM PULSE PAIR)	215	JORWAY	1	/75		12,1037
N	,131	CLOCK GENERATOR(INTERN 1MHZ, EXT 10MHZ, 7 DECADES 1HZ-1MHZ TTL O/P,5USEC WIDTH)	730A	POLON	1	/74		12,1038
N	,131	INTERVAL TIMER/WATCHDOG (100USEC-300SEC INTERVAL, 1 SEC--100 SEC TIMEOUT)	EC 384	SENSION	1			12,1039
N	,131	REAL TIME CLOCK (PRESET COUNTER, PRESET TIMER 3,8USEC TO 18,2 HRS, ELAPSE TIME)	RTC 018	STND ENGINEERING	1	/74	(12)	12,1040

NCD	CODE	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	RS. REF.
N	,132	DORNIER MODULES ALSO MARKETED BY SIEMENS		SIEMENS				12,1041
N	,132	OUTPUT REGISTER (12 CHANNEL)	OR 612	STND ENGINEERING	1	/73		12,1042
N	,132	OUTPUT REGISTER (12BIT)	PR 312	STND ENGINEERING	1	/73		12,1043
N	,132	OUTPUT REGISTER (24BIT)	PR 314	STND ENGINEERING	1	/73		12,1044
N	,133	8 CHANNEL TIMED TRIAC OUTPUT	3040	KINETIC SYSTEMS	2	/74		12,1045
N	,133	OUTPUT REGISTER (16BIT,250V/,1A MAX, 2X37-WAY O/P CONN)	360A	POLON	1	/73		12,1046
N	,133	(SAME, 25V/1A MAX)	360B		1	/73		
N	,142	INPUT/OUTPUT REGISTER (24BIT)	IO 302	STND ENGINEERING	1	02/75		12,1047
N	,143	INTERFACING INPUT UNIT (8BIT DATA/STATUS & CONTR REGS, FOR FACIT SP1 INTERFACE)		ARSYCOM	1	/74	(12)	12,1048
N	,143	INTERFACING OUTPUT UNIT(8BIT DATA, CONTR & STATUS REGS, FOR FACIT SP1 INTERFACE)		ARSYCOM	1	/74	(12)	12,1049
N	,143	TELETYPE OR CRT INTERFACE	TCO 100	STND ENGINEERING	1	/74		12,1050
N	,144	DISPLAY SYNCHRONIZING (COMPATIBLE WITH 50HZ 625 LINE MONITORS)	3200E	KINETIC SYSTEMS	1	/74	(12)	12,1051
N	,144	COLOUR DISPLAY INTERFACE	9062	NUCL. ENTERPRISES	NA	04/75	(12)	12,1052
N	,145	ADC-CAMAC INTERFACE (FOR PULSE ADC 8215, 8210,8211,8212,8112 & T-O-F CONV 8270)	5910	LABEN	1		(12)	12,1053
N	,151	NIM FANOUT (7-ORED INPUTS, 8 O/P+2 COMPL O/P GATED FROM DATAWAY)	216	JORWAY	1	/75		12,1054
N	,151	DUAL HIGH SPEED GATE(4X4 NIM INPUTS)	2 HSG 2062	SEN	1		(12)	12,1055
N	,153	BCD TO BINARY CONVERTER (29BIT BCD TO 24BIT BINARY, CONV TIME 325 NSEC)	CD 001	STND ENGINEERING	1	/73	(12)	12,1056
N	,153	BINARY TO BCD CONVERTER (CONV TIME 325 NSEC,24BITS TO MAX 16777216-1 BCD CODED)	CD 002	STND ENGINEERING	1	/73	(12)	12,1057
N	,154	CAMAC CORE MEMORY MODULE (2K X 16 BIT)	MM 216C	STND ENGINEERING	3	/74	(12)	12,1058
N	,154	(4K X 16 BIT)	MM 416C		3	/74	(12)	
N	,154	(8K X 16 BIT)	MM 816C		3	/74	(12)	
N	,154	(2K X 24 BIT)	MM 224C		3	/74	(12)	
N	,154	(4K X 24 BIT)	MM 424C		3	/74	(12)	
N	,161	OCTAL ADC (8X11BIT + OVF, POS INPUT, 1 MV RESOL, COMMON STROBE, FAST CLEAR)	AD811	FG&G/ORTEC	1	03/75		12,1059
N	,161	OCTAL TDC (8X11BIT+OVF, COMMON START, 100PSEC RESOLUTION, FAST CLEAR)	TD811	EG&G/ORTEC	1	03/75		12,1060
N	,161	SINGLE 10BIT ANALOG TO DIGITAL CONVERTER	3515S	KINETIC SYSTEMS	1	/74		12,1061
N	,161	SINGLE 12BIT ANALOG TO DIGITAL CONVERTER	3520S	KINETIC SYSTEMS	1	/74		12,1062
N	,161	12-CHANNEL PEAK ADC (10BIT/CH, I/P THR, COMMON FAST CLEAR & INHIB, NIM)	2259	LRS-LECROY	1	/74	(12)	12,1063
N	,161	FAST ADC(10 & 12BIT VERSIONS,WITH SAMPLE AND HOLD, CONV TIME 2USEC/4.5USEC)	FADC 2067	SEN	2		(12)	12,1064
N	,161	FAST DUAL ADC (DATA AS FOR 2067)	2 FADC 2068		2		(12)	
N	,161	DUAL ADC (14BIT, 50USEC CONV TIME)	A/D 114	STND ENGINEERING	1	03/75		12,1065
N	,161	DUAL ADC (10BIT, 10USEC CONV TIME)	A/D 210	STND ENGINEERING	2	03/75		12,1066
N	,161	DUAL ADC (12BIT, 25USEC CONV TIME)	A/D 212	STND ENGINEERING	2	03/75		12,1067
N	,161	HIGH SPEED DIGITIZER (6BIT, 100NSEC, RESOLUTION, WITH 256 WORD BUFFER)	SA/D 01	STND ENGINEERING	1	/74	(12)	12,1068
N	,161	OCTAL TIME TO DIGITAL CONVERTER	TD 008	STND ENGINEERING	1	04/75		12,1069
N	,164	FET MULTIPLEXER (16 CHANNELS, MAX +OR-10V, DATAWAY SET + INCR ADDRESS)	DO 200-1031	DORNIER	1	/72		12,1070
N	,164	(SAME WITH FRONT PANEL CONNECTOR)	DO 200-1231		1	/72		
N	,164	RELAY MULTIPLEXER (32 CHANNELS)	750	POLON	2	03/75		12,1071
N	,164	MULTIPLEXER 32X2 CONTACTS	C 72468-A0628-A001	SIEMENS	1	/74		12,1072
N	,164	MULTIPLEXER 16X4 CONTACTS		SIEMENS	1	/74		12,1073
N	,164	SOLID STATE MULTIPLEXER (16 CH, RANDOM, & SEQUENT ACCESS, MULTI-MUX SCAN MODE)	MX 016	STND ENGINEERING	1	/74	(12)	12,1074
N	,165	PROGRAMMABLE AMPLIFIER (GAIN 1, 10, 100, 1000)	DO 200-1054	DORNIER	1	05/75		12,1075
N	,165	(SAME BUT DUAL CHANNEL VERSION)	DO 200-1055		1	05/75		
N	,165	ACTIVE FILTER AMPLIFIER(10 - 1000 GAIN, .25-4USEC GAUSS. PULSE SHAPING,0-10V OUT	1101	POLON	3	/74		12,1076
N	,165	BASELINE RESTORER(,1% COUNT RATE STABIL UP TO 50KHZ,0-10 I/O SIGNALS,1V/V GAIN)	1102	POLON	2	/74		12,1077

NCD	CODE	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	RS. REF.
N	,165	DELAY AMPLIFIER(,25 - 4,75USEC DELAY, 0 TO 10V IN/OUT SIGNALS, 1V/V GAIN)	1103	POLON	2	03/75		12,1078
N	,165	SUM-INVERT AMPLIFIER(,2% NON-LINEARITY, 1V/V GAIN, 0 TO 10V IN/OUT SIGNALS)	1104	POLON	1	/74		12,1079
N	,165	LINEAR RATEMETER (10 TO 100K CPS RANGE, 1S TO 30S TIME CONSTANTS)	1301	POLON	3	/74		12,1080
N	,165	CAMAC CONTROLLED PULSE SHAPER (4 PM I/P, 4 NIM I/P & 6 NIM O/P)	CPS 2065	SEN	1		(12)	12,1081
N	,168	DUAL PULSE DELAY UNIT	PD 002	STND ENGINEERING	5	/73		12,1082
N	,17	DETECTOR BIAS SUPPLY (0 TO +/-2000V, 1MOHM AND 10MOHM OUTPUT RESISTANCE)	1901	POLON	4	/74		12,1083
N	,211	PRIME COMPUTER BRANCH DRIVER	1260	BI RA SYSTEMS	NA	/74		12,2001
N	,211	PRIME COMPUTER BRANCH DRIVER (WITH DMT CHANNEL)	1260-1		NA	/74		
N	,211	BRANCH HIGHWAY DRIVER	3991	KINETIC SYSTEMS	2	/75		12,2002
N	,211	NOVA BRANCH DRIVER	NBD 100	STND ENGINEERING	2	/74		12,2003
N	,212	CONTROLLER/INTERFACE FOR T1600 COMPUTER (MAX 8 CRATES, PROG/ADDR,SCAN/STOP MODE)	JCT 16-10	NUMELEC	2			12,2004
N	,212	DMA MODULE	JDM 16,10		2			
N	,213	SINGLE CRATE CONTROLLER/PDP-11 INTERFACE (PROGRAMMED TRANSFERS, WITH NAF REG &	CA-11-FP	D E C	2	06/75		12,2005
N	,213	CONNECTOR TO DMA OPTION CA-11-FN)						
N	,213	PDP-11 DMA INTERFACE FOR CA-11-FP (8 DMA CHANNELS, MI OR LIST MODE, 16BIT WC, CA,	CA-11-FN		2	06/75		
N	,213	OFFSET FOR EACH CHANNEL, LIMIT REGISTER)						
N	,213	SINGLE CRATE CONTROLLER FOR PDP-8/E ADDR,-SCAN MODE, DMA I/O, MAX 22 LAMS)		EISENMANN	0			12,2006
N	,213	INTERFACE FOR HP 2114-2115 COMPUTERS, COMPRISING--		NUCL. ENTERPRISES				12,2007
N	,213	16-BIT CONTROLLER AND	9030		3	/72	(7)	
N	,213	INTERFACE CARD FOR HP 2114-2115	CS 0058			/74		
N	,213	INTERFACE FOR HONEYWELL 316-516 COMPUTERS, COMPRISING--		NUCL. ENTERPRISES				12,2008
N	,213	16-BIT CONTROLLER AND	9030		3	/72	(7)	
N	,213	INTERFACE CARD FOR HONEYWELL 316-516	CS 0057			/74		
N	,214	CADET (SINGEL-CRATE CONTROLLER FOR READ-ONLY SYSTEM, INCL MODULE TEST & DISPLAY)	CT 2058	SEN	4		(12)	12,2009
N	,214	PRINT BUFFER (ALLOWS A PARALLEL PRINTER TO BE USED WITH THE CT 2058)	PB 2059		0		(12)	
N	,214	CAMAC MICROPROCESSOR CRATE CONTROLLER	MIK XA	STND ENGINEERING	0	/74		12,2010
N	,217	CONTROL DATA 6000 SERIES SYSTEM DRIVER (USE WITH 3960)	3973	KINETIC SYSTEMS	3	/75		12,2011
N	,22	TRANSF, ISOLATED SERIAL D-PORT ADAPTER	3932	KINETIC SYSTEMS	1	/75		12,2012
N	,22	DRIVER FOR SERIAL HIGHWAY (WITH 256 WORD FIFO BUFFER)	3994	KINETIC SYSTEMS	4	/75		12,2013
N	,232	LAM GRADER (24BIT MASK REG, WITH CABLE, PATCHABLE C-ADDR-REG FOR MULTI-CRATE BG)	C 76451-A18-A1	SIFMENS	0	/74		12,2014
N	,321	CAMAC SYSTEM SIMULATOR/TESTER	CSS/T	STND ENGINEERING	6	/73		12,3001
N	,341	BUFFERED EXTENDER (25NSEC PROPAGATION DELAY, 60 CM FLEXIBLE CABLE)	060	POLON	1	03/75		12,3002
N	,341	DATAWAY EXTENDER MODULE	FB 01	STND ENGINEERING	1	/72		12,3003
N	,341	PROLONGATEUR POUR TIROIRS CAMAC NON CABLE (UNWIRED EXTENDER)	41402	TRANSRACK	1	/70		12,3004
N	,411	VOLTAGE REGULATOR (+&-6V 25A MAX, OR 40A MAX WITH EXTERNAL +6V SUPPLY)	1923	BORER		/74		12,4001
N	,411	POWER CRATE (9070 CRATE WITH 9022 POWER SUPPLY)	9071	NUCL. ENTERPRISES	24	/74	(12)	12,4002
N	,411	POWERED CAMAC CRATE	PCS/12	STND ENGINEERING	25	/72		12,4003
N	,411	POWERED CAMAC CRATE	PCS/42	STND ENGINEERING	25	/72		12,4004
N	,412	CRATE	9070	NUCL. ENTERPRISES	24	/74		12,4005
N	,413	CAMAC CRATE (+6V/25A,-6V/12,5A,+&-24V/6A,+&-12V/4A)	DO 200-3001	DORNIER	NA	/74		12,4006
N	,413	(SAME WITHOUT +&-12V SUPPLY)	DO 200-3002		NA	/74		
N	,417	CARD EXTENDER (FOR SUPPLY OF 2057)	CE 2061	SEN				12,4007
N	,417	CHASSIS CAMAC NORMALISE 5U (EMPTY CRATE,360 MM DEEP)	40206	TRANSRACK	25	/74		12,4008
N	,417	(*=7 FOR 460MM & *=8 FOR 525MM DEEP)	4020*		25			

NCD	CODE	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	RS. REF,
N	,417	CHASSIS CAMAC 5U UTILES (EMPTY CRATE,6U TOTAL,360MM DEEP,VENTILATION HARDWARE)	40203	TRANSRACK	25	/74		12,4009
N	,417	(*-4 FOR 460MM & *-5 FOR 525MM DEEP)	4020*		25			
N	,417	CHASSIS CAMAC 5U UTILES (EMPTY CRATE,6U TOTAL,360MM DEEP,WITH TWO FANS)	40200	TRANSRACK	25	/74		12,4010
N	,417	(*-1 FOR 460MM & *-2 FOR 525MM DEEP)	4020*		25			
N	,422	CAMAC POWER SUPPLY	1510/12	STND ENGINEERING	NA	/72		12,4011
N	,422	CAMAC POWER SUPPLY	1510/42	STND ENGINEERING	NA	/72		12,4012
N	,432	ADDRESS & FUNCTION DECODING PC	AFD 2066	SEN				12,4013
N	,432	DATAWAY MOTHERBOARD ASSEMBLY	DM 2	STND ENGINEERING		/72		12,4014
N	,433	KLUGE BOARD FOR WIRE WRAP	15	JORWAY	3	/74		12,4015
N	,433	TIROIRE MODULAIRE POUR CARTE BASCULANTE (EMTY MODULE FOR HINGED CARD)	41405	TRANSRACK	2	/72		12,4016
N	,433	TIROIRE MODULAIRE POUR 2 CARTES BASCUL, (EMTY MODULE FOR 2 HINGED CARDS)	41406		3	/72		
N	,437	NIM ADAPTOR	9072	NUCL. ENTERPRISES		/74		12,4017

CORRECTED ITEMS

NCD	CODE	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	RS. REF,
C	,111	QUAD CAMAC SCALER (4X16BIT OR 2X32BIT, 100MHZ)	1004A	BORER	1	01/75		12,1084
C	,111	12-CHANNEL 100 MHZ SCALER(12X24BIT,-0,5V I/P THR, COMMON FAST CLEAR & INHIB, NIM)	2551	LRS-LECROY	1	/74	(12)	12,1085
C	,121	INPUT GATE (2X24BIT STATIC DATA,INTEGR FOR 1USEC,TTL LEVELS, 2X37-WAY I/P CONN)	321	POLON	1	/74		12,1086
C	,122	DORNIER MODULES ALSO MARKETED BY SIEMENS		SIEMENS				12,1087
C	,127	STATUS INTERRUPT (24BIT,I/P&LATCH&LAM& MASK,GROUP&SEL-LAM-TEST,VAR.LOGIC&LEVEL)	C-SI-24	WENZEL ELEKTRONIK	1	/74	(12)	12,1088
C	,131	CLOCK/TIMER (0,001S TO 10 HRS TIME INTERVAL,TIME-OF-DAY OUTPUT)	1411	BORER	1	/72	(3)	12,1089
C	,132	OUTPUT REGISTER (24BIT WORD, TTL O/P VIA 37-WAY CONN)	351	POLON	1	/73		12,1090
C	,133	OUTPUT REGISTER (16BIT, 48V/,05A MAX, 2X37-WAY O/P CONN)	360	POLON	1	/73		12,1091
C	,142	UNIVERSAL INPUT/OUTPUT REGISTER	SPS 2090	NUCL. ENTERPRISES	1	01/75	(12)	12,1092
C	,143	TELETYPE INTERFACE (FOR ASR 33, SER I/O)	500	POLON	1	/74		12,1093
C	,143	CASSETTE INTERFACE (READS & WRITES BY 8 OR 16BIT WORDS, 8BIT LAM REG) CONTROLS--	J CK 10	SCHLUMBERGER	1	/75	(12)	12,1094
C	,143	CASSETTE DRIVER FOR 1 CASSETTE	C CK 10			/75	(12)	
C	,143	CASSETTE DRIVER FOR 2 CASSETTES	C CK 11			/75	(12)	
C	,144	DISPLAY SYNCHRONIZING (COMPATIBLE WITH 60HZ 525 LINE MONITORS)	3200	KINETIC SYSTEMS	1	/71		12,1095
C	,144	COLOR MONITOR	RGB 5200 M	KINETIC SYSTEMS		/71		12,1096
C	,145	STEPPING MOTOR CONTROLLER, ACCELERATING	3361	KINETIC SYSTEMS	1	/73		12,1097
C	,145	INTERFACE CAMAC-TO-LABEN 8000SERIES MULTICHANNEL ANALYZERS	5380	LABEN	3		(12)	12,1098
C	,147	FORMAT-SYNCHRONIZER (IDENT & S/P OF DATA WORDS, SOFT- & HARDWARE PROGRAMMABLE)	DO 200-2260	DORNIER	4	/73		12,1099
C	,147	SERIAL INTERFACE (V24 SPEC, QUAD VERSION VARIABLE TRANSMISSION RATES)	9045	NUCL. ENTERPRISES	1	/73		12,1100
C	,153	DECIMAL INPUT 6 NUMBERS 3 DIGITS CODE CONVERTER	DO 200-2005	DORNIER	2	/74		12,1101
C	,154	PROGRAMMABLE READ ONLY MEMORY (32 WORDS, 18 BITS, LOADED BY SOLDER CONNECTIONS)	221	POLON	1	03/75		12,1102
C	,161	QUAD CAMAC SCALER (4X16BIT OR 2X32BIT, 100MHZ)	1004A	BORER	1	01/75		12,1103
C	,161	ANALOG INPUT (DUAL SLOPE ADC, +/-16V RANGE,14BITS/16V+SIGN,0,2SEC CONVERSION)	DO 200-1021	DORNIER	1	/72		12,1104
C	,162	DUAL DAC (12BIT, +AND-10V OR +AND-20MA)	C 76451-A15-A4	SIEMENS	1	/73		12,1105
C	,164	RELAY MULTIPLEXER(16 CHANNELS, MAX 200V/ 500MA OR 10VA, DATAWAY SET+INCR ADDRESS)	DO 200-1036	DORNIER	1	/72		12,1106
C	,164	(WITH FRONT PANEL CONNECTOR)	DO 200-1236		1	/72		
C	,164	(SAME WITH LOW THERMO VOLTAGE CONTACTS)	DO 200-1035		2	/71		
C	,164	(WITH FRONT PANEL CONNECTOR)	DO 200-1235		2	/71		
C	,165	PROGRAMABLE AMPLIFIER/ATTENUATOR (GAIN 0DB TO 60DB IN 10 STEPS, ATTENUATION ,5)	DO 200-1052	DORNIER	2	/73		12,1107
C	,165	(SAME BUT DUAL CHANNEL VERSION)	DO 200-1053		1	/73		
C	,165	LINEAR GATE (,2% NON-LINEARITY, +/- 1V/V GAIN, 0 TO 10V IN/OUT SIGNALS)	1105	POLON	1	/73		12,1108

NCD	CODE	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	RS. REF.
C	,165	PULSE STRETCHER(,05-,9USEC I/P WIDTH, 1USEC O/P WIDTH OF PULSES, .9 V/V GAIN)	1106	POLON	1	/74		12,1109
C	,165	SINGLE CHANNEL ANALYSER (,2-10V LO/HI LEVEL, ,2-2V WINDOW, ,5-2,5USEC DELAY)	1201	POLON	3	/74		12,1110
C	,165	LOGIC SHAPER AND DELAY (,2 TO 110USEC DELAY, ,2 TO 11USEC O/P PULSE WIDTH)	1401	POLON	2	/74		12,1111
C	,165	UNIVERSAL COINCIDENCE (,1 TO 2USEC RESOLVING TIME)	1402	POLON	2	/74		12,1112
C	,165	FAN OUT (1 NIM IN, 2 NIM & 1 COMPL TTL OUT)	1504	POLON	1	/73		12,1113
C	,213	SINGLE CRATE CONTROLLER TO HP COMPUTERS WITH EXT SYNCHRONISATION FACILITIES	1531A	BORER	2	02/75		12,2015
C	,213	SINGLE CRATE CONTROLLER/PDP-11 INTERFACE (MULTIPLE BUS ADDRESS VERSION)	CA-11-E	D E C	2	/74	(9)	12,2016
C C	,213 ,213	INTERFACE FOR K202 COMPUTER (24BIT,AUTO- NOMOUS BLOCK TRANSFERS TO/FROM MEMORY, L-NUMBER INTERRUPT ENCODER)	100	POLON	3	/73		12,2017
C C	,214 ,214	DATA PROCESSOR (AUTONOMOUS PROGRAMABLE SINGLE DATAWAY CONTROLLER 16 REGISTERS, REGISTERS AND MEMORY EXPANDABLE)	DO 200-2951	DORNIER	3	/73		12,2018
C	,311	TEST CONTROLLER WITH PROGRAM PLUGBOARD	SPS 2048	NUCL. ENTERPRISES	2	01/75	(12)	12,3005
C	,331	DATAWAY SERVICE MODULE	J DS 10	SCHLUMBERGER	1	/74	(12)	12,3006
C	,331	CONTROLEUR SORTIE DATAWAY (DATAWAY TEST MODULE)	41403	TRANSRACK	1	/70		12,3007
C	,341	PROLONGATEUR POUR TIROIRS CAMAC CABLE (WIRED EXTENDER)	41401	TRANSRACK	1	/70		12,3008
C	,411	POWERED CRATE (6U,VENTILATED,NO FAN,130W +6V/15A,-6V/4A,+AND-24V/2A,+200V/50MA)	015	POLON	25	/71		12,4018
C	,411	POWERED CRATE(SEE P7 ALJ 13)	C7 ALJ 13 DW	SAPHYMO-STEL	25		(1)	12,4019
C	,411	POWER SUPPLY (CAMAC CRATE)	CM5125/53/DW/BLOCS	SAPHYMO-STEL	25	/72		12,4020
C	,411	COMPLETE POWER CRATE	CPC 2057	SEN	25	/74	(11)	12,4021
C C	,412 ,412	UNPOWERED CRATE WITH DATAWAY (360 MM) (525 MM)	CM 5125/33/DW CM 5125/53/DW	SAPHYMO-STEL	25 25			12,4022
C	,417	UNPOWERED CRATE	UC 2057	SEN	25	/74	(11)	12,4023
C	,417	VENTILATION MODULE	VM 2057	SEN		/74	(11)	12,4024
C	,421	POWER SUPPLY SYSTEM (CRATE) (MODULE OPTIONS AS FOLLOWS)	C4BMT204/C6BMT306	SAPHYMO-STEL		/72		12,4025
C	,421	POWER SUPPLY MODULE 6 V/10 A (6V/20A & 6V/40A OPTIONS ALSO AVAILABLE)	BP 75 6,10					
C	,421	12 V/ 2 A (ALSO 12V/4A, 7A, 15A & 25A OPTIONS)	BSN					
C	,421	24 V/ 1,2A (ALSO 24V/2,5A, 3,5A, 9A & 15A OPTIONS)	BSN					
C	,422	POWER SUPPLY (BACK MOUNTING,+6V/15A, -6V/4A,+AND-24V/2A,+200V/50MA,130W)	CZC-10	POLON		/73		12,4026
C	,422	POWER SUPPLY UNIT -MAINTENANCE ONLY- (+6V/10A,-6V/2A,+AND-24V/1,5A)	P4 ALJ 13	SAPHYMO-STEL		/71		12,4027
C	,422	(+6V/5A,-6V/1,5A,+AND-12V/1,5A, +AND-24V/1,5A) -MAINTENANCE ONLY-	P6 ALJ 13					
C	,422	(+6V/25A,-6V/10A,+AND-12V/3A, +AND-24V/3A,+200V/0,1A,MAX 200W)	P7 ALJ 13	SAPHYMO-STEL				12,4028
C	,422	POWER SUPPLY (+6V/32A,-6V/32A,+24V/6A, -24V/6A,+200V/,1A,300W, POWER FAIL LAM)	PS 2057	SEN		/74	(11)	12,4029
C	,432	DATAWAY MINI WRAPPING (MOTHERBOARD WITH 25 DATAWAY CONNECTORS)	J/DW	SAPHYMO-STEL		/71		12,4030
C	,433	PRINTED CIRCUIT TEST BOARD	10	JORWAY	1	/71		12,4031
C	,433	TIROIR MODULAIRE DE COMMANDE (SUPPLY CONTROL MODULE)	41703	TRANSRACK	1	/70		12,4032

DELETED ITEMS

D	,111	OCTAL SCALER (12BITS,8 INPUTS,50MHZ,EACH	S812	EG&G/ORTEC	1	/71
D	,111	QUAD SCALER TYPE 003 (4X16BIT,50MHZ)	S003	EG&G/ORTEC	1	/73
D	,113	DUAL PRESET SCALER (2X16BIT,5MHZ,	PS016	EG&G/ORTEC	1	/73
D	,114	REAL TIME CLOCK, LIVE TIME INTEGRATOR,	RC014	EG&G/ORTEC	1	/73
D	,117	DUAL INCREMENTAL POSITION ENCODER	PE019	EG&G/ORTEC	1	/73
D	,123	INTERRUPT REGISTER 12-INPUT & STROBE	IR026	EG&G/ORTEC	1	/73
D	,124	WORD GENERATOR (SWITCH REGISTER,12BIT)	WG005	EG&G/ORTEC	1	/73

NCD	CODE	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	RS. REF.
D	,127	INTERRUPT REQUEST REGISTER (8BIT, TTL	7013=1	NUCL. ENTERPRISES	1	/70		
D	,132	NIM FAST LOGIC DRIVER (12 OUTPUTS)	ND027	EG&G/ORTEC	1	/73		
D	,133	DRIVER (24BIT OUTPUT REGISTER,SET AND	9013	NUCL. ENTERPRISES	1	/71		
D	,143	MAG TAPE DRIVER(9=TRACK NRZI COMPATIBLE	308,100	EDS SYSTEMTECHNIK	3	/74		
		1 TO 4K 8=BIT DATA BUFFER)						
D	,143	B.S.INTERFACE READER (8BIT DATA + PARITY	7057=1	NUCL. ENTERPRISES	1	/71		
D	,143	B.S.INTERFACE DRIVER (8BIT DATA + PARITY	7058=1	NUCL. ENTERPRISES	1	/71	(1)	
D	,144	DISPLAY POINT PLOTTER	PP012	EG&G/ORTEC	1	/73		
D	,144	DISPLAY DRIVER (INTERFACE FOR TEKTRONIX	DD015		1	/73		
D	,144	CHARACTER GENERATOR	CG018		1	/73		
D	,144	DISPLAY VECTOR GENERATOR	VG028		1	/73		
D	,144	INDICATOR (1X16BIT OR 2X8BIT,INDICATES	9014	NUCL. ENTERPRISES	1	/71		
D	,145	WIRE DETECTOR SCANNER(64X16BIT MEMORY	WCS=200	NANO SYSTEMS	1	/72	(5)	
D	,145	SCANNER TEST MODULE	WCS=201	NANO SYSTEMS	1	/72	(5)	
D	,145	CONTROLLER=INTERFACE FOR DIGITAL SCOPE	APD/R7912	TEKTRONIX	2	/74		
D	,147	CONTROLLED TIMER (BUSY=DONE LOGIC)	CT021	EG&G/ORTEC	1	/73		
D	,152	HEX IL2 TO IL1 CONVERTER	7051=1	NUCL. ENTERPRISES	1	/70		
D	,152	QUIN L1 TO IL1 CONVERTER(5 HARWELL STAN=	7053=1	NUCL. ENTERPRISES	1	/70		
D	,161	DUAL DIGITAL VOLTMETER (2X10BIT, DIFF	DV013	EG&G/ORTEC	1	/73		
D	,161	QUAD TIME DIGITIZER (SPARK CHAMBER	TD031	EG&G/ORTEC	1	. /73		
D	,161	ANALOGUE TO DIGITAL CONVERTER (12BIT,	7055=1	NUCL. ENTERPRISES	1	/70		
D	,162	DIGITAL TO ANALOGUE CONVERTER	7015	NUCL. ENTERPRISES	1	/70		
D	,162	DUAL DAC (12BIT, +AND=10V)	C 76451=A15=A3	SIEMENS	1	/73	(6)	
D	,211	PDP=9 CAMAC INTERFACE	CA 15 A/PDP=9	D E C	NA	/71		
D	,212	DATAWAY CONTROLLER DDP=516(PART OF 7000=	7022=1	NUCL. ENTERPRISES	4	/70		
D	,231	CRATE CONTROLLER TYPE D (CONFORMS TO EUR	DO 200=2901	DORNIER	2	/71		
D	,233	TERMINATOR MODULE	TC024	EG&G/ORTEC	2	/71		
D	,411	CAMAC MINICRATE		EDS SYSTEMTECHNIK	17	/73		
D	,411	POWER CRATE (7005=2 CRATE WITH	9023	NUCL. ENTERPRISES	24	/71	(2)	
D	,411	POWERED CRATE(SEE P4 ALJ 13)	C4 ALJ 13 D	SAPHYMO=STEL	25	/71	(1)	
D	,411	POWERED CRATE(SEE P6 ALJ 13)	C6 ALJ 13 D		25		(1)	
D	,411	POWER SUPPLY (CAMAC CRATE)	CM5125/53/AW/BIP	SAPHYMO=STEL	25			
D	,412	CRATE	7005=2	NUCL. ENTERPRISES	24	/70		
D	,412	UNPOWERED CRATE WITH DATAWAY ( )	CM 5125/33/AW	SAPHYMO=STEL	25	/71		
D	,412	( )	CM 5125/53/AW		25			
D	,417	FAN UNIT (FOR ALB/10 SUPPLY SYSTEM)	VALB/10	SAPHYMO=STEL		/72		
D	,417	CRATE BLOWER UNIT		STND ENGINEERING			(5)	
D	,417	CAMAC CRATE (EMPTY CRATE)	CS	STND ENGINEERING	25			
D	,417	CHASSIS CAMAC NORMALISE 5U	CM 5025 30	TRANSRACK	25	/70		
D	,417	(XX=40 FOR 460MM & =50 FOR 525MM DEEP)	CM 5025 XX		25			
D	,417	CHASSIS CAMAC 5U UTILES (EMPTY CRATE,6U	CM 5125 30	TRANSRACK	25	/70		
		TOTAL,360MM DEEP,VENTILATION HARDWARE)						
D	,417	(XX=40 FOR 460MM & =50 FOR 525MM DEEP)	CM 5125 XX		25			
D	,417	CHASSIS CAMAC 5U UTILES (EMPTY CRATE,	CM 5125 31	TRANSRACK	25	/70		
D	,417	(XX=41 FOR 460MM & =51 FOR 525MM DEEP)	CM 5125 XX		25			
D	,417	CHASSIS CAMAC 5U UTILES (EMPTY CRATE,6U	CM 5125 32	TRANSRACK	25	/70		
D	,417	(XX=42 FOR 460MM & =52 FOR 525MM DEEP)	CM 5125 XX		25			
D	,421	SUPPLY CHASSIS 2KW	ALB/10	SAPHYMO=STEL		/73	(2)	
		(RAW SUPPLY FOR REGULATOR MODULES)						
D	,421	FAN UNIT	VALB/10					
D	,421	WIRED RACK 42 U	BC 42					
D	,421	POWER SUPPLY MODULE 6 V 5 A(REGULATOR)	BPR 605					
		(ALSO 6V/10A&25A, 12V/2A&5A, 24V/3A&5A)						
D	,433	GENERAL PURPOSE IC PATCHBOARD (MAX 33	CAMAC CG 164	GSPK	NA	/70	(2)	
D	,437	NIM ADAPTOR	7009=2	NUCL. ENTERPRISES	NA	/70		

INDEX OF MANUFACTURERS

AEG-Telefunken
Elisabethenstrasse 3, Postfach 830
D-7900 Ulm, Germany

AMP AG
Haldenstrasse 11
CH-6000 Luzern, Switzerland

C Applied Computer Systems Ltd.
2 Charltonstreet,
Manchester M1 3JL, England

N Arsycom B.V.
Kabelweg 43-47,
Amsterdam 1016, Netherland

BF Vertrieb GmbH
(Sales of F & H Products in Germany)
Bergwaldstrasse 30, Postfach 76
D-7500 Karlsruhe 41, Germany
See also Frieseke & Hoepfner

BI RA Systems, Inc.
3520 D Pan American Freeway, N.E.
Albuquerque, New Mexico 87107, USA

Borer Electronics AG
Postfach
CH-4500 Solothurn 2, Switzerland

Burndy Electra AG
Hertistrasse 23,
CH-8304 Wallisellen, Switzerland

Cannon Electric GmbH
Bureau Schweiz
Friedenstrasse 15,
CH-8304 Wallisellen, Switzerland

Carr Fastener Co. Ltd.
Cambridge House,
Nottingham Road, Stapleford,
Nottinghamshire, England

Digital Equipment Corporation (DEC)
146 Main Street, Maynard
Massachusetts 01754, USA

N Digital Equipment GmbH
D-8000 München 40
Wallensteinplatz 2, Germany

Dornier System
Vertrieb Elektronik, Abt. VÇE
Postfach 648
D-799 Friedrichshafen, Germany

EDS Systemtechnik GmbH
Trierer Strasse 281
D-5100 Aachen, Germany

EG & G/ORTEC, Inc.
High Energy Physics Department
500 Midland Road, Oak Ridge,
Tennessee 37830, USA

J. Eisenmann, Elektronik für
Prozessautomatisierung
Vogesenstrasse 6
D-7501 Blankenloch-Büchig,
Germany

Elliott — See GEC-Elliott

Emihus Microcomponents Limited
Belgian Branch,
Res. Hera — Appt. No. 64,
Passage International, 29
B-1000 Bruxelles, Belgium

Emihus Microcomponents Limited
Clive House
12-18 Queens Road, Weybridge,
Surrey, England

FRB Connectron
3-5, Rue des Tilleuls,
F-92600 Asnières, France

Frieseke & Hoepfner GmbH
Export Dept. & Production
Tennenloher Strasse
D-8520 Erlangen-Brück, Germany

See also BF Vertrieb
(Sales of F & H Products in Germany)

GEC-Elliott Process Automation Ltd.
Camac Group, New Parks
Leicester LE3 1UF, England

General Automation International
1055 South East Street, Anaheim,
California 92805, USA

Grenson Electronics Limited
Long March Industrial Estate
High March Road, Daventry
Northants NN11 4HQ, England

Hans Knuerr KG
Ampfingstrasse 27
D-8000 München 8, Germany

High Energy & Nuclear Equipment SA
2, Chemin de Tavernay,
CH-1218 Grand-Saconnex,
Switzerland

Hytec Electronics
225 Courthouse Road, Maidenhead,
Berkshire, England

IDAS (Informations-, Daten -und
Automationssysteme) GmbH
Kornmarkt 9
D-6250 Limburg/Lahn, Germany

Imhof-Bedco Ltd.
Colne Way Trading Estate, By-Pass,
Watford, Herts, England

Informatek
Z.A. de Courtaboeuf, B.P. 81
F-91401 Orsay, France

ITT Cannon — See Cannon

J and P Engineering (Reading) Ltd.
Portman House
Cardiff Road, Reading
Berkshire RG1-8JF, England

Joerger Enterprises
32 New York Avenue
Westbury, N.Y. 11590, USA

Jorway Corporation
27 Bond street, Westbury,
New York 11590, USA

Kinetic Systems Corporation
Maryknoll Drive,
Lockport, Ill. 60441, USA

Knuerr — See Hans Knuerr

Laben (Division of Montedel)
Via Edoardo Bassini, 15
I-20133 Milano, Italy

LeCroy Research Systems Corp.
126 North Route 303, West Nyack,
New York 10994, USA

LeCroy Research Systems SA
81, Avenue Casai
CH-1216 Cointrin, Geneva
Switzerland

N LeCroy Research Systems Ltd.
74 High Street, Wheatley,
Oxfordshire OX9 1XP, England

Lemo SA
CH-1110 Morges, Switzerland

Leonische Drahtwerke AG
Abholfach
D-8500 Nürnberg 1, Germany

LRS-LeCroy — See LeCroy

Nuclear Enterprises Limited
Bath Road, Beenham
Reading RG7 5PR, England

Nuclear Specialties Inc.
6341 Scarlett Court, Dublin,
California 94566, USA

Nucletron SA
11, Chemin G. De Prangins
CH-1004 Lausanne, Switzerland

N Numelec S.A.
Division Electronique Nucléaire
2, Petite Place,
F-78000 Versailles, France

ORTEC GmbH
Frankfurterring 81
D-8000 München 40, Germany

N ORTEC Incorporated
Software Dev, Digital Data Systems
100, Midland Road, Oak Ridge,
Tennessee 37830, USA

O.S.L.
18bis, Avenue du Général de Gaulle
F-06340 La Trinité, France

OSL/Willsher and Quick — See OSL
Respectively Willsher and Quick

Packard Instrument Company, Inc.
Subsidiary of AMBAC Industries, Inc.
2200 Warrenville Rd.,
Downers Grove, Illinois 60515, USA

Philips N.V., Dep. Elcoma
Interconnection Group, Building BA
Eindhoven, Netherlands

Polon
Nuclear Equipment Establishment
00-086 Warsaw, Bielanska 1, Poland

Polon — See also Zjednoczone

Power Electronics (London) Limited
Kingston Road Commerce Estate
Leatherhead, Surrey, England

Precicable Bour
151, Rue Michel-Carre
F-95101 Argenteuil, France

RDT, Ing. Rosselli Del Turco
Rossello S.L.R.
Via di Tor Cervara, 261
Roma Nomentano
I-00155 Rome, Italy

SABCA — See Emihus,
Belgian Branch

Saip — See Schlumberger

C Saphymo-Stel
51, rue de l'Amiral-Mouchez
F-75013 Paris, France

Schlumberger Instruments &
Systèmes
Dépt. Instrumentation Nucléaire
B.P. 47 (57, rue de Paris)
F-92222 Bagneux, France

Semra-Benney (Electronics) Limited
Industrial Estate,
Chandler's Ford, Eastleigh,
Hampshire SO5 3DP, England

SEN Electronique
31, Avenue Ernest-Pictet, C.P. 57
CH-1211 Genève 13, Switzerland

N Sension Limited
2 Brooklands Drive, Goostrey, Crewe
Cheshire CW4 8JB, England

Siemens AG
Bereich Mess- und Prozesstechnik
Postfach 21 1080
D-7500 Karlsruhe 21, Germany

SOCAPEX (Thomson-CSF)
9, Rue Edouard Nieuport
F-92153 Suresnes, France

N Software Partners
Grossgerauer Weg 2
D-61 Darmstadt, Germany

Souriau et Cie
13, Rue Gallieni, B.P. 410
F-92 Boulogne-Billancourt, France

Standard Engineering Corporation
44800 Industrial Drive,
Fremont, California 94538, USA

Tech and Tel — See Technograph

Techcal — See Stnd Engineering

Technograph and Telegraph Ltd.
Easthamstead Road,
Bracknell, Berkshire, England

Tekdata Limited
Westport Lake, Canal Lane,
Tunstall, Stoke-on-Trent,
Staffs ST6 4PA, England

Telefunken — See AEG-Telefunken

Transrack
B.P. 12
22, Avenue Raspail
F-94100 Saint-Maur, France

Ultra Electronics (Components) Ltd.
Fassetts Road, Loudwater,
Bucks. HP10 9UT, England

Vero Electronics Ltd.
Industrial Estate, Chandler's Ford,
Eastleigh, Hants SO5 3ZR, England

Karl Wehrmann, Industrievertr.
Spaldingstrasse 74
D-2000 Hamburg 1, Germany

Wenzel Elektronik
Wardeinstrasse 3
D-8000 München 82, Germany

Wenzel Elektronik (UK) Ltd.
Arndale House, The Precinct,
Egham, Surrey, England

Willsher and Quick Ltd.
Walrow, Highbridge
Somerset, England

Willsher and Quick GmbH
Steylerstrasse 27, Postfach 2192
D-4054 Nettetal 2, Germany

Zjednoczone Zaklady Urzadzen
Jadrowych Polon, Biuro Zbytu
00-086 Warsaw, Bielanska 1, Poland

CAMAC SOFTWARE PRODUCTS GUIDE

INTRODUCTION

The Software Products Section of the CAMAC Products Guide lists a number of software packages, programs and routines which have been developed by software firms, manufacturers of CAMAC equipment, and at research laboratories.

Work is going on to implement IML — the intermediate level CAMAC language. One contribution to IML implementation is listed below, but at least five other laboratories are at present engaged in implementing IML on several computers.

The products listed below are either in current use or will be so in the nearest few months. Some of the software listed is commercially available, information about other is presumably available from respective authors. The correctness of each entry has been carefully checked against data provided.

Inclusion in the list does not necessarily indicate endorsement, recommendation or approval by the ESONE Committee, nor does omission indicate disapproval.

The classification used tentatively and reproduced below, is the same as was proposed in the March 1974 issue (No. 9) of this Bulletin.

SOFTWARE CLASSIFICATION GROUPS

.50 Fundamental Concepts, General Subjects

READER SERVICE	REF 12.5001
CLASS CODE -	.50
TITLE- - - -	IMPLEMENTING CAMAC BY COMPILERS
AUTHOR(S)- -	W. KNEIS, GFK, ZYKLOTRON-LB., KARLSRUHE, GERMANY
PUBL. REF. -	PROC CAMAC SYMPOS, LUXMBG, DEC 1973

DESCRIPTION--
DEMANDS ON REAL-TIME SYSTEMS SUCH AS MINIMUM EXECUTION TIME MINIMUM CORE REQUIREMENTS, ETC., RECOMMEND THE USE OF COMPILERS IN PROGRAMMING, THE POSSIBILITY TO IMPLEMENT A CAMAC LANGUAGE BY A COMPILER IS FIRST OF ALL A FUNCTION OF THE LEVEL AND CONCEPT OF THE LANGUAGE. META-LANGUAGES, THE SYNTAX OF A PROGRAMMING LANGUAGE, ARE USED TO FORMULATE A COMPILER FOR A SPECIFIC LANGUAGE. THE METHOD DESCRIBED HAS BEEN USED TO WRITE A COMPILER FOR IML, THE INTERMEDIATE LEVEL CAMAC LANGUAGE, IMPLEMENTED IN AN ASSEMBLER ENVIRONMENT.

READER SERVICE	REF 12.5002
CLASS CODE -	.50
TITLE- - - -	PROCEDURE CALLS - A PRAGMATIC APPROACH
AUTHOR(S)- -	J. MICHELSON, H. HALLING, KFA, JUELICH.
PUBL. REF. -	PROC CAMAC SYMPOS, LUXMBG, DEC 1973
ESONE REGSTR DATE	31 MAY 1974

DESCRIPTION--*
DISCUSSION OF PROCEDURE CALLS AS THE BASIS FOR CAMAC SOFTWARE WITHIN HIGH-LEVEL LANGUAGES. COMPARISON WITH SYNTAX MODIFICATIONS TO LANGUAGES. DISCUSSION OF IMPLEMENTATION RESTRICTIONS DUE TO LANGUAGE REQUIREMENTS FOR EXISTING HIGH-LEVEL LANGUAGES, E.G. CLOSED SYSTEM-SUBROUTINES WHICH EXECYCLES AS A GROUP). COMPARISON OF US-NIM CAMAC FORTRAN CUTE ONE DEFINED OPERATION (INVOLVING ONE OR MORE CAMAC SUBROUTINES AND PROCEDURE-CALL SYNTAX OF FSONF SWG IML LANGUAGE. APPLICATION OF PROCEDURE-CALLS TO APPLICATION-ORIENTED SOFTWARE.

CORR**************	CORRECTED, REVISION A
READER SERVICE	REF 12.5003
CLASS CODE -	.501(PL-11)
TITLE- - - -	CAMAC FACILITIES IN THE PROGRAMMING LANGUAGE OF PL-11
AUTHOR(S)- -	ROBERT D RUSSELL, CERN, GENEVA
PUBL. REF. -	PROC CAMAC SYMPOS, LUXMBG, DEC 1973 YELLOW REPORT, CERN 74-24, DEC 1974
NAME/ACRONYM -	EXTENDED PL-11
OPERATIVE DATE-	1971/72
COMPUTER -	PDP-11, WORD LENGTH 16 BITS
INTERFACE(S) -	CA-11 (EG&G/ORTEC)
SOFTWARE TYPE -	LANGUAGE, PL-11(EXTENDED)
INCORP TECHNIQUE	IN-LINE CODING OF CAMAC STATEMENTS
FACILITIES -	SYMBOLIC DEVICE NAME USED DEMAND HANDLING IS INCLUDED

DESCRIPTION--
PL-11 IS AN INTERMEDIATE-LEVEL, MACHINE-ORIENTED PROGRAMMING LANGUAGE EXTENDED TO INCLUDE CAMAC FEATURES. SYNTACTIC FORM OF CAMAC STATEMENTS ARE ANALOGOUS TO STANDARD PL-11 STATEMENTS. SYMBOLIC NAMES FOR VARIABLES AND FUNCTIONS ARE DECLARED AT ONCE, AND OPERATIONS ARE EXECUTED BY STATEMENTS REFERRING TO THESE NAMES. USE OF SYMBOLIC NAMES MAKES PROGRAMS READABLE, AND SIMPLIFIES MODIFICATIONS OF CAMAC CONFIGURATIONS.
EXAMPLE OF STANDARD STATEMENT--
WHILE PRINTSTATUS = BUSY DO
EXAMPLE OF CAMAC STATEMENT--
WHILE CRTSTATUS = BUSY DO

READER SERVICE	REF 12.5004
CLASS CODE -	.501 (CATY)
AUTHOR(S)- -	F R GOLDING, DARESBURY LABORATORIES
NAME/ACRONYM -	CATY
COMPUTER -	ANY
SOFTWARE TYPE -	LANGUAGE

DESCRIPTION- -
CATY IS A MACHINE INDEPENDENT HIGH-LEVEL LANGUAGE BASED UPON A SUBSET OF BASIC WITH EXTENSIONS FOR ADDRESSING CAMAC. PROGRAMS WRITTEN IN CATY ARE COMPILED AND NOT INTERPRETED. THUS, THE SPEED OF OPERATION WHEN CAMAC IS TESTED UNDER CATY IS COMPARABLE WITH THE SPEED OF OPERATION IN APPLICATIONS. CATY HAS BEEN IMPLEMENTED ON PDP-11 (SEE .543).

NEW***************	NEW ENTRY
READER SERVICE	REF 12.5005
CLASS CODE -	.501 (IML)
TITLE- - - -	THE DEFINITION OF IML A LANGUAGE FOR USE IN CAM C SYSTEMS
PREPARED BY -	ESONE COMMITTEE, SOFTWARE W.G. AND AEC NIM COMMITTEE, SOFTWARE W.G.
PUBL. REF. -	REPORT ESONE/IML/01, OCT 1974, AND REPORT TID-26615, JAN 1975
NAME/ACRONYM -	IML
MAINTENANCE BY-	ESONE COMMITTEE IN COLLABORATION WITH NIM COMMITTEE
OBTAINABLE FROM	ESONE SECRETARIAT AND U.S. GOVERNMENT PRINTING OFFICE RESPECTIVELY
ESONE REGSTR DATE	AUG/SEPT 1974
COMPUTER -	ANY
SOFTWARE TYPE -	LANGUAGE

DESCRIPTION--
IML IS A LANGUAGE USED TO EXPRESS THE OPERATIONS DESCRIBED IN THE CAMAC HARDWARE SPECIFICATIONS, AND THEIR INTERACTION WITH A COMPUTER SYSTEM. IML STATEMENTS LINK CAMAC STRUCTURES AND MODES OF OPERATION TO DATA STRUCTURES AND REAL-TIME FEATURES IN THE COMPUTER SYSTEM.
THIS DEFINITION IS A GUIDE FOR THOSE IMPLEMENTING LANGUAGES AND OPERATING SYSTEMS WHO WISH TO MAKE CAMAC INPUT/OUTPUT AVAILABLE TO USERS. FEATURES ARE INCLUDED WHICH SUPPORT THE CAMAC BRANCH HIGHWAY AND THE CAMAC SERIAL HIGHWAY.
THE LANGUAGE IS DEFINED SEMANTICALLY - THE SYNTAX USED TO EXPRESS IML DEPENDS ON THE ENVIRONMENT. THE MACRO SYNTAX IML-M1 IS DEFINED IN AN APPENDIX.

.51 User-Oriented Programs I (full system support)

READER SERVICE	REF 12.5006
CLASS CODE -	.51
TITLE- - - -	CAMAC OPERATING SYSTEM FOR CONTROL APPLICATIONS
AUTHOR(S)- -	DR B. MERTENS, IKP, KFA, JUELICH
PUBL. REF. -	CAMAC BULLETIN NO 9, MARCH 1974
NAME/ACRONYM -	COS
AVAILABLE ON/AS	PAPER TAPE, ASCII CODE
OPERATIVE DATE-	1972
COMPUTER -	PDP-15, CORE REQUIREMENTS- 16K
INTERFACE(S) -	TYPE 2200 (BORER)
SOFTWARE TYPE -	SYSTEM PROGRAM
LANGUAGE -	FORTRAN & MACRO-ASSEMBLER
CAMAC FACILITIES	SYMBOLIC DEVICE NAMES USED, SINGLE & MULTIPLE ACTION PER INSTRUCTION, REAL/TIME DEMEND HANDLING INCORPORATED

DESCRIPTION--
THE SYSTEM SOFTWARE PACKAGE PERMITS READ AND WRITE OF UP TO 100 MODULES. REAL-TIME TASKS MAY BE DEFINED ON-LINE. ABOUT 60 ELEMENTARY COMMANDS ARE PRE-DEFINED, SUCH AS--
-NAME MODULE/C=1, N=2, A=3/DEFINE SYMBOLIC NAME
-READ MODULE/F=0
-WRITE MODULE 321/F=16
-DISAB MODULE/F=24
-DEFINE TASK/OPEN A TASK-DEFINITION
-END/CLOSE TASK-FILE
-AFTER 15 SECS TASK/EXECUTE USER-DEFINED TASK
-15 SECS FROM NOW
-SOLL MODULE 3456/VALUE TO BE WRITTEN NEXT TO MODULE

READER SERVICE	REF 12.5007
CLASS CODE =	.51
TITLE= = = =	BACKGROUND=FOREGROUND SYSTEM FOR PULSE=HEIGHT ANALYSIS OF TWO= DIMENSIONAL MULTIWIRE PROPORTIONAL CHAMBER DATA
AUTHOR(S)= =	DR A HEUSLER, IPK, KFA, JUELICH
NAME/ACRONYM =	BFG
AVAILABLE ON/AS	PAPER TAPE, ASCII CODE
OPERATIVE DATE=	1974?
COMPUTER =	PDP=15, CORE REQUIREMENTS = 24K
INTERFACE(S) =	TYPE 2200 (BORER)
MIN SYSTEM CONFIG	MAGTAPE, DECTAPE, DISK, & MEMORY SCANNING DISPLAY (IN=HOUSE)
SOFTWARE TYPE =	SYSTEM PROGRAM
LANGUAGE =	FORTRAN & MACRO=ASSEMBLER

DESCRIPTION==
THE SYSTEM SOFTWARE PERMITS START AND STOP OF BLOCK TRANSFER FROM THE A/D CONVERTERS TO THE PDP=15 MEMORY (LIST MODE OUTPUT ONTO MAGTAPE ON=LINE SORTING IF DESIRED).
THE BORER INTERFACE HAS BEEN MODIFIED TO ALLOW BLOCK LENGTHS UP TO 4K 18 BIT WORDS.

READER SERVICE	REF 12.5008
CLASS CODE =	.51
TITLE= = = =	TRIUMF CONTROL SYSTEM SOFTWARE
AUTHOR(S)= =	D. P. GURD, W. K. DAWSON, TRIUMF, UNIVERSITY OF ALBERTA, CANADA
PUBL. REF. =	CAMAC BULLETIN NO 5, NOVEMBER 1972
OPERATIVE DATE=	1973
COMPUTER =	4 SUPERNOVAS
INTERFACE(S) =	IN=HOUSE TYPE
SOFTWARE TYPE =	FULL SYSTEM SUPPORT FOR CONTROL OF TRIUMF CYCLOTRON

DESCRIPTION==
THE SYSTEM SOFTWARE PACKAGE MONITORS OVER 1000 ANALOGUE PARAMETERS AND 1000 DIGITAL STATUS POINTS, SEARCHES OUT=OF= LIMIT READINGS, DISPLAYS MEASUREMENTS ON REQUEST,
SETS OVER 300 ANALOGUE POINTS FROM A CENTRAL CONSOLE AND PERFORMS A NUMBER OF OTHER ROUTINES.
A REAL=TIME EXECUTIVE PROGRAM = NATS (FOR NOVA ASYNCHRONOUS TASKING SUPERVISOR) = SCHEDULES AND SUPERVISES CAMAC TASKS, SUPPORTED BY A SUBPROGRAM LIBRARY, AS THEY ARE REQUESTED.
JOBS TO BE PERFORMED ARE STRUCTURED INTO SEQUENCES OF CAMAC OPERATIONS SPECIFIC TO A PIECE OF HARDWARE (= CAMAC MODULE). THERE IS THUS A DIRECT MODULAR HARDWARE=SOFTWARE CORRESPOND= ENCE. CONTROL IS BASICALLY CLOCK=INITIATED SOFTWARE SCAN OF CYCLOTRON MONITORING, BUT INTERRUPTS ARE INCLUDED, MAINLY INITIATED BY CONSOLE.

READER SERVICE	REF 12.5009
CLASS CODE =	.51
AUTHOR(S)= =	D GURD, TRIUMF,UNIV. ALBERTA,CANADA
NAME/ACRONYM =	CAMAC
OPERATIVE DATE=	1973
SOFTWARE TYPE =	SYSTEM SOFTWARE

DESCRIPTION= =
THE SYSTEM SOFTWARE= CAMAC = CONSISTS OF SEVERAL SUBROUTINE CALLS. THESE ARE= =
PRIMITIVE SUBROUTINES PERFORMING THE ACTUAL I/O OPERATIONS, MODULE SUBROUTINES, THE MUX/ADC SUBROUTINES, CAMAC LAMS OR INTERRUPTS, SERIAL TASKS, AND AN INTERPRETER (FOR DATA).

.52 User-Oriented Programs II (specific run-time programs)

NEW***************	NEW ENTRY
READER SERVICE	REF 12.5010
CLASS CODE =	.52
TITLE= = = =	OPERATING SYSTEM SOFTWARE PACKAGES
NAME/ACRONYM =	SEE DESCRIPTION
MAINTENANCE BY=	DEC
OBTAINABLE FROM	DEC (SEE INDEX OF MANUFACTURERS)
OPERATIVE DATE=	1975
COMPUTER =	PDP=11
INTERFACE(S) =	SEE DESCRIPTION
SOFTWARE TYPE =	CAMAC SERVICE ROUTINES, USER=, INTERFACE= & DESCRIPTOR PROGRAMS

DESCRIPTION==
THE SOFTWARE PACKAGES ARE COMPLETE OPERATING SYSTEMS. CONTROLLERS AND OPERATING SYSTEMS ARE RELATED AS FOLLOWS==
CA=11=C USES RSX=11=D OPERATING SYSTEM
CA=11=E USES RSX=11=M OR RT=11
CA=11=F USES RSX=11=M OR RT=11

.53 User-Oriented Programs III (subprograms, etc.)

READER SERVICE	REF 12.5011
CLASS CODE =	.53 (BASIC)
TITLE= = = =	CAMAC AND INTERACTING PROGRAMMING
AUTHOR(S)= =	DR E M RIMMER, CERN, GENEVA
PUBL. REF. =	PROC CAMAC SYMPOS, LUXMBG, DEC 1973 & BASIC CALLABLE ROUTINES, NP GROUP NOTE, NP=DHG, CERN
NAME/ACRONYM =	HPCMA, HPCMB, HPCMC
MAINTENANCE BY=	DR E M RIMMER
OBTAINABLE FROM	NP DIV, CERN, CH=1211 GENEVA
AVAILABLE ON/AS	PAPER TAPE, ASCII CODE
OPERATIVE DATE=	1971/72
COMPUTER =	H=P 2100=SERIES, 8K 16 BIT WORDS
INTERFACE(S) =	2201(BORER), 7218 & HPCC=066(CERN)
MIN SYSTEM CONFIG	TTY OR TEK 4010 TERMINAL & CC=A1
SOFTWARE TYPE =	SET OF SUBROUTINES
LANGUAGE =	HP ASSEMBLY
HOST LANGUAGE =	BASIC (NP EXTENSION OF)
CAMAC FACILITIES	IN=LINE CODED CALLS IN BASIC, SUBROUTINES IN ASSEMBLY, ABS ADDR
FACILITIES =	SINGLE & MULTIPLE ACTION PER INSTRUCTION, NO DEMAND HANDLING

DESCRIPTION= =
THESE BASIC=CALLABLE CAMAC SUBROUTINES IN THREE VERSIONS FOR THREE INTERFACES PROVIDE MOST COMMAND FACILITIES FOR CONTROL AND DATA TRANSFER. DATA WORDS MAY BE 16 OR 24 BITS LONG (ONLY 16 BITS FOR HPCC=066), BINARY, BCD OR LOGIC (0 OR 1). ROUTINES COVER BLOCK TRANSFERS, PROGRAMMED AND SEQUENTIAL ADDRESSING & UTILITY ROUTINES, IN TOTAL 18 & 3 OPTIONALLY.
GENERAL FORM OF CALL STATEMENT==
= = =CALL (SUBROUTINE NUMBER,C,N,A,F,D,Q)
= = =CALL (SUBROUTINE NUMBER,C,N,A,F,D(I),Q,W)
WHERE W IS WORD COUNT, D IS DATA, C,N,A,F, & Q HAVE USUAL MEANING
EX== CALL(10,1,2,0,16,D(I),Q,20)
TIME IS APPR 5 MSECS/STATEMENT, BLOCK TRANSFER CALL GENE= RATED DIRECTLY BY INTERFACE ARE MUCH FASTER.

READER SERVICE	REF 12.5012
CLASS CODE =	.53(FORTRAN)
TITLE= = = =	SPECIFICATIONS FOR STANDARD CAMAC SUBROUTINES
AUTHOR(S)= =	RICHARD F THOMAS JR.
PUBL. REF. =	CAMAC BULLETIN NO 6, MARCH 1973
NAME/ACRONYM =	SEE DESCRIPTION
OBTAINABLE FROM	USAEC NIM COMMITTEE, CAMAC SWG
AVAILABLE ON/AS	ALGORITHM
OPERATIVE DATE=	1973
COMPUTER =	INDEPENDENT, MEMORY SIZE NOT SPEC.
INTERFACE(S) =	ANY
SOFTWARE TYPE =	SET OF SUBROUTINES
LANGUAGE =	FORTRAN
CAMAC FACILITIES	FUNDAMENTAL CAMAC OPERATIONS, STANDARD BLOCK TRANSFERS IN SINGLE & MULTIPLE ACTION STATEMENTS

DESCRIPTION= =
A SET OF 6 SUBROUTINES, OF WHICH ONE IS CALLED BY ALL THE OTHER PERMITS A GREAT VARIETY OF SINGLE AND MULTIPLE CAMAC OPERATIONS TO BE PERFORMED. DEMAND HANDLING, OTHER THAN BY TEST LAM, IS NOT COVERED.
THE SUBROUTINES EXECUTE CAMAC OPERATIONS AS FOLLOWS==
CMCBSC = SINGLE CAMAC FUNCTION AT SINGLE ADDRESS ONE OR MORE TIMES
CMCSEQ = SINGLE CAMAC FUNCTION AT SUCCESSION OF ADDRESSES
CMCASC = SPECIFIED CAMAC FUNCTION IN ADDRESS SCAN MODE
CMCRPT = SPECIFIED CAMAC FUNCTION IN REPEAT MODE
CMCSTP = SPECIFIED CAMAC FUNCTION IN STOP MODE
CMCLUP = SPECIFIED CAMAC FUNCTION AT A HIERARCHICAL SEQUENCE OF ADDRESSES WITH OPTIONAL SKIP OF SEQUENCE BASED ON Q.
GENERAL FORM OF STATEMENT==
CALL CMC... (PARAMETER LIST)
EXAMPLE== CALL CMCSTP (F,B,C,N,AD,LN,DATA,ERRORA,NEX)

CORR***************	CORRECTED, REVISION A
READER SERVICE	REF 12.5013
CLASS CODE -	.53
TITLE- - - -	CAMAC FUNCTION FOR RT11
AUTHOR(S)- -	L BYARS, R KEYSER
NAME/ACRONYM -	CAMAC, CAMINT
VERSION- - -	RT11
MAINTENANCE BY-	ORTEC
OBTAINABLE FROM	ORTEC (SEE INDEX OF MANUFACTURERS)
AVAILABLE ON/AS	PAPER TAPE
OPERATIVE DATE-	1974
COMPUTER -	PDP-11
INTERFACE(S) -	DC011 (EG&G/ORTEC)
SOFTWARE TYPE -	SUBROUTINES
LANGUAGE -	PDP-11 ASSEMBLY
HOST LANGUAGE -	RT11/FORTRAN
INCORP TECHNIQUE	CALLS TO FORTRAN LIBRARY ROUTINES
CAMAC FACILITIES	SINGLE OR MULTIPLE INSTRUCTIONS, DEMAND HANDLING

DESCRIPTION- -
THIS SOFTWARE PACKAGE CONSISTS OF A NUMBER OF SUBROUTINES FOR FORTRAN/RT11 CALLING CAMAC FUNCTIONS.
THE CAMAC CALL STATEMENT HAS THE FOLLOWING FORM--
CALL CAMAC (IF, IN, IA, IQ, IDATA).
THEY ARE USED TO TRANSFER DATA TO/FROM CAMAC AND FOR TEST PURPOSES.
IF, IN, IA ARE RESPECTIVELY FUNCTION, STATION ADDRESS AND SUBADDRESS, IQ IS BOTH QBIT AND XBIT.
CAMINT IS USED TO HANDLE INTERRUPTS FROM CAMAC CRATE, AND HAS THE GENERAL FORM--
CAMINT(IN,NAME1)
WHERE IN IS THE STATION NUMBER AND NAME1 IS THE NAME OF THE SUBROUTINE TO BE EXECUTED WHEN THE INTERRUPT OCCURS.

READER SERVICE	REF 12.5014
CLASS CODE -	.53(FORTRAN)
TITLE- - - -	FORTRAN SUBROUTINES
AUTHOR(S)- -	H POHL
NAME/ACRONYM -	FORTRAN CALLS
VERSION- - -	V002
OBTAINABLE FROM	H POHL, ZEL, KFA, JUELICH
AVAILABLE ON/AS	DECTAPE
OPERATIVE DATE-	MARCH 1972
COMPUTER -	PDP-11, 16K 16 BIT WORDS MEMORY
INTERFACE(S) -	TYPE 1533A (BORER)
SOFTWARE TYPE -	PROCEDURE CALLS
LANGUAGE -	FORTRAN ON PDP-11 (THREADED CODE)
INCORP TECHNIQUE	IN-LINE SUBROUTINE CALLS
CAMAC FACILITIES	SINGLE ACTION STATEMENTS

DESCRIPTION- -
FORTRAN SUBROUTINES FOR SINGLE ACTIONS. MUCH SIMPLER THAN THE NIM APPROACH (REF. R. F. THOMAS) FOR THE BORER 1533A CONTROLLER WRITTEN IN RE-ENTRANT CODE.

CORR***************	CORRECTED, REVISION A
READER SERVICE	REF 12.5015
CLASS CODE -	.53(FORTRAN)
AUTHOR(S)- -	J M STEPHENSON, L A KLAISNER
NAME/ACRONYM -	KSCLIB
OBTAINABLE FROM	KINETIC SYSTEMS (SEE INDEX OF MFRS)
OPERATIVE DATE-	1974
COMPUTER -	PDP-11, 16K CORE MEMORY REQUIRED
INTERFACE(S) -	TYPES 3911A, 3991 & 3992 (KINETIC)
LANGUAGE -	FORTRAN
SOFTWARE TYPE -	LIBRARY OF FORTRAN FUNCTIONS AND SUBROUTINES

DESCRIPTION- -
THIS SOFTWARE PACKAGE IMPLEMENTS THE CMCBSC SERIES OF STANDARD FORTRAN CALLS DESCRIBED IN CAMAC BULLETIN NO 6, 1973. IT ALSO INCLUDES THE BIT MANIPULATION FUNCTIONS EXCLUSIVE OR, INCLUSIVE OR, AND, NOT, & SHIFT. THE PACKAGE SUPPORTS UP TO 8 CRATES INTERFACED THROUGH MODEL 3911A UNIBUS *) CRATE CONTROLLERS, UP TO 7 CRATES PER 3991 BRANCH DRIVER AND UP TO 61 CRATES PER 3992 SERIAL BRANCH DRIVER. THE NUMBER OF PARALLEL AND SERIAL BRANCHES SHOULD BE LESS THAN 8.

*) UNIBUS IS A TRADE MARK OF DIGITAL EQUIPMENT CORP.

READER SERVICE	REF 12.5016
CLASS CODE -	.53
TITLE- - - -	I/O MACROS FOR CAMAC
AUTHOR(S)- -	D STUCKENBROCK, G KLENERT, SIEMENS AG, KARLSRUHE
NAME/ACRONYM -	MACAM
OBTAINABLE FROM	SIEMENS (SEE INDEX OF MFRS)
AVAILABLE ON/AS	PAPER TAPE, CARDS & SOURCE DECK
OPERATIVE DATE-	NOVEMBER 1974
COMPUTER -	PR 320/330
INTERFACE(S) -	CC 320 & SC 330 (SIEMENS)
MIN MEMORY SPACE	1K OF 16 BITS (SUPERVISOR EXCL)
MIN SYSTEM CONFIG	TTY AND SUPERVISOR PROGRAM
SOFTWARE TYPE -	I/O ROUTINES
ENVIRONMENT FOR -	CAMAC SOFTWARE IS ASSEMBLER 300
LANGUAGE -	MACROS - ASSEMBLER,CALLS - FORTRAN
FACILITIES -	CONCURRENT MULTI-USER OPERATION, SYSTEM RUNS UNDER REAL-TIME SUPERVISOR

DESCRIPTION- -
A SET OF I/O MACRO SUBROUTINES CAN BE CALLED BY ANY USER PROGRAM CONCURRENTLY RUNNING ON THE COMPUTER, PROVIDED THEY OPERATE UNDER A REAL-TIME SUPERVISOR PROGRAM. THE ROUTINES COMPRISE THE FUNCTIONS READ, WRITE, AND EXECUTION OF CONTROL COMMANDS. BLOCK TRANSFERS ARE PERFORMED ON CONSTANT OR VARIABLE CAMAC ADDRESS, AND IN INCREMENT MODE OR RANDOM-LIST MODE. THE COORDINATION OF USER PROGRAMS AND CAMAC PROVIDED BY THE SUPERVISOR, FACILITATES GREATLY THE LAM HANDLING. THE SYSTEM ALLOWS UP TO 32 CONCURRENTLY OPERATING USER PROGRAMS AND UP TO 8 BRANCHES WITH - IN ALL - 24 CRATES. SYSTEM SOFTWARE ENVIRONMENTS FACILITATE INCORPORATION OF THE SUBROUTINE CALLS AS STATEMENTS EMBEDDED IN FORTRAN PROGRAMS.

.54 Support Software I (translators)

READER SERVICE	REF 12.5017
CLASS CODE -	.54
TITLE- - - -	S/UNIP AN UNIVERSAL MACRO PROCESSOR
AUTHOR(S)- -	SOFTWARE-PARTNERS
MAINTENANCE BY-	SOFTWARE-PARTNERS
OBTAINABLE FROM	SAME, (SEE INDEX OF MANUFACTURERS)
OPERATIVE DATE-	APRIL 1974
SOFTWARE TYPE -	MACRO PROCESSOR
LANGUAGE -	WRITTEN IN HIGH LEVEL LANGUAGE
COMPUTER -	CAN RUN ON IBM, UNIVAC, CDC,ICL, SIEMENS, ETC.
CAMAC FACILITIES	INCORPORATED IN-LINE FOR FULL-SET IML WITH MACRO PROCESSOR DIRECTIVES

DESCRIPTION- -
S/UNIP IS A LANGUAGE INDEPENDENT MACRO PROCESSOR AND THEREFORE A TOOL FOR MACRO EXPANSION OF EVERY EXISTING OR OR FUTURE PROGRAMMING LANGUAGE. THUS S/UNIP MAINTAINS AND PROCESSES MACROS IN HIGH LEVEL LANGUAGES (FORTRAN, BASIC, ALGOL, PEARL, ETC.) AS WELL AS ASSEMBLY LANGUAGES. S/UNIP OPERATES AS A PRE-PROCESSOR GENERATING SOURCE CODE STATEMENTS FOR SUBSEQUENT COMPILATION, POSSIBLY ON ANOTHER COMPUTER.

NEW***************	NEW ENTRY
READER SERVICE	REF 12.5018
CLASS CODE -	.541
TITLE- - - -	A MACRO ASSEMBLER FOR TYPE MBD-11 MICROPROGRAMMED BRANCH DRIVER
COMPUTER -	PDP-11
OBTAINABLE FROM	BI RA SYSTEMS (SEE INDEX OF MFRS)
SOFTWARE TYPE -	MACRO ASSEMBLER (TRANSLATOR)
INTERFACE(S) -	MBD-11 (BI RA SYSTEMS)

DESCRIPTION--
THE MACRO ASSEMBLER HAS BEEN DEVELOPED TO FACILITATE THE WRITING OF PROGRAMS FOR THE MBD-11 MICROPROCESSOR-INTERFACE. THE ASSEMBLER TRANSLATES PROGRAMS WRITTEN IN MACRO CODE INTO INSTRUCTIONS ACCEPTABLE BY THE MBD-11. UP TO 16 INSTRUCTIONS CAN BE STORED IN THE MBD-11. INSTRUCTIONS ARE MICRO-STRUCTURED TO FORM A POWERFUL SET OF INSTRUCTIONS.

READER SERVICE	REF 12.5019
CLASS CODE -	.541(MACRO11)
TITLE- - - -	MACROS FOR 1533A
AUTHOR(S)- -	MR. HEER
NAME/ACRONYM -	MACRO 1533A
MAINTENANCE BY-	MR. HEER
OBTAINABLE FROM	MR. HEER, ZEL, KFA, JUELICH
AVAILABLE ON/AS	DECTAPE
OPERATIVE DATE-	FEBRUARY 1973
COMPUTER -	PDP-11, MIN 8K 16 BIT WORDS
INTERFACE(S) -	TYPE 1533A (BORER)
MIN SYSTEM CONFIG	DOS V004, 008, 009
SOFTWARE TYPE -	MACRO-SET
LANGUAGE -	MACRO 11
CAMAC FEATURES-	ARE INCORPORATED IN-LINE
ENVIRONMENT FOR -	CAMAC SOFTWARE IS ASSEMBLER
CAMAC FACILITIES	SINGLE ACTION STATEMENTS, SYMBOLIC DEVICE NAMES

DESCRIPTION- -
THIS IS A SIMPLE MACRO SET (NO DECLARATIONS) FOR SINGLE ACTION STATEMENTS. EXECUTION SPEED IS HIGHER (APPROX 30 MICROSECS PER INSTRUCTION, DEPENDING ON TYPE OF INSTRUCTION ON TYPE OF PDP-11). NOT INTERRUPTABLF MACROS (PRIORITY=7)

NEW***************	NEW ENTRY
READER SERVICE	REF 12.5020
CLASS CODE -	.541(IML)
TITLE- - - -	MACRO-IML IMPLEMENTATIONS FOR DEC PDP-11 COMPUTERS
AUTHOR(S)- -	M KUBITZ, R KIND, HMI-BERLIN
PUBL. REF. -	CAMAC BULLETIN NO 12, APRIL 1975
OBTAINABLE FROM	M KUBITZ, BEREICH D/E, HMI-BERLIN GERMANY
AVAILABLE ON/AS	ALL MEDIA
OPERATIVE DATE-	1974
COMPUTER -	PDP-11, 16K, 24K, 44K, OR 52K
INTERFACE(S) -	CA-11A (DEC, 1533A (BORER)
MIN SYSTEM CONFIG	DOS V08/09, RSX-11D
SOFTWARE TYPE -	MACRO SET OF IML (IMPLEMENTED)
LANGUAGE -	PDP-11 ASSEMBLY
CAMAC FEATURES-	INCORPORATED BY MACROS
CAMAC FACILITIES	FULL SET OF IML-MACROS INCLUDING DEMAND HANDLING

DESCRIPTION--
IML IS TMPLFMENTED ON PDP-11 IN ACCORDANCF WITH THE MACRO SYNTAX AS DEFINED IN THE DOCUMENT ESONE/IML/01 (SEE CLASS .501 ABOVF). VERSIONS ARF AVAILABLE FOR INTERFACE-CONTROLLERS AND DEC OPERATING SYSTEMS AS MENTIONED IN THE LEFT COLUMN.
IMPLEMENTATION COVERS THE FULL SET OF IML MACROS AND DEMAND HANDLING EXCEPT BLOCK TRANSFER ON SPECIAL LAM, X-FRROR CONTROL STATEMENTS, AND SUBSCRIPT MODE. TRANSFER MODES NOT IMPLEMENTED BY HARDWARE ARE SIMULATED BY SOFTWARE.
I/O TRANSFER INSTRUCTIONS ARE EMBEDDED IN THE MACROS AND ARE PFRFORMED DIRECTLY IN ACTION BY THE MACROS.
ADDRESS CALCULATION AT ASSEMBLY TIME GIVES OPTIMIZED
ADDRESS CALCULATION AT ASSEMBLY TIME GIVES OPTIMUM RUN TIME CODE. HOST LANGUAGES CAN BE PDP-11 MACRO ASSEMBLER OR FORTRAN (VIA SUBROUTINE CALL).
MEMORY REQUIREMENTS VARY WITH OPERATING SYSTEM AND IF FULL SET IS NEEDED, OR A SUB-SET IS ACCEPTABLE. 16K IS REQUIRED FOR A SUB-SET WITH DOSV08/09, 52K FOR FULL SET AND RSX11D.

READER SERVICE	REF 12.5021
CLASS CODE -	.543
TITLE- - - -	A BASIC MACRO-11 COMPILER
AUTHOR(S)- -	B BECKS
PUBL. REF. -	CAMAC BULLETIN NO 10, JULY 1974
NAME/ACRONYM -	MABA
MAINTENANCE BY-	B BECKS
OBTAINABLE FROM	B BECKS, ZEL, KFA, JUELICH
AVAILABLE ON/AS	DECTAPE
OPERATIVE DATE-	JANUARY 1974
COMPUTER -	PDP-11, 16K 16 BIT WORDS OF MEMORY
INTERFACE(S) -	TYPE 1533A (BORER)
MIN SYSTEM CONFIG	DOS V08 OR V09, 16K
SOFTWARE TYPE -	COMPILER
LANGUAGE -	BASIC
INCORP TECHNIQUE	IN-LINE
ENVIRONMENT FOR -	CAMAC SOFTWARE IS MACRO ASSEMBLER
CAMAC FACILITIES	SINGLE ACTION STATEMENTS

DESCRIPTION- -
THIS COMPILER TRANSLATES TESTFD (INTERPRETIVE) BASIC PROGRAMS INTO MACRO-11 SOURCE CODE. RUN TIME IS IMPROVED BY A FACTOR OF 15 TO 20. EASILY ADAPTABLE TO OTHER CONTROLLERS (MACROS).
OUTPUT CODE LINKED WITH FLOATING POINT PACKAGE CAN RUN ON STAND-ALONE MINI-COMPUTERS.

READER SERVICE	REF 12.5022
CLASS CODE -	.543(CATY)
TITLE- - - -	A CAMAC TESTING AID FOR USE ON PDP-11
AUTHOR(S)- -	F R GOLDING, APPLIED COMPUTER SYST.
NAME/ACRONYM -	CAT11
OBTAINABLE FROM	APPLIED COMPUTER SYSTEMS LTD, WENZEL ELEKTRONIK, NUCL ENTERPRISES, GEC-ELLIOTT (SEE INDEX OF MFRS)
OPERATIVE DATE-	1973
COMPUTER -	PDP-11, 4K OR 8K MEMORY REQUIRED DEPENDING ON VERSION
INTERFACE(S) -	EXECUTIVE SUITE (GEC-ELLIOTT), C-CSC-11 (WENZEL), 9030 (N.E.)
MIN SYSTEM CONFIG	CONTROL VISTA, READER, PUNCH
SOFTWARE TYPE -	SYSTEM (EXECUTIVE, COMPILER ETC)
LANGUAGE -	CATY (BASED ON BASIC)

DESCRIPTION- -
USERS TEST PROGRAMS ARE TYPED IN AND THEREAFTER COMPILED AND RUN. IT IS POSSIBLE TO EDIT THE PROGRAM AND RERUN IT WITH-OUT HAVING TO RFTYPE THE ORIGINAL PROGRAM. CAMAC COMMANDS ARE EMBEDDED IN PROGRAM AS STATEMENT LINES.
CAT11 HAS INTERRUPT AS SYSTEM FEATURE, THE USER MAY TYPE HIS OWN INTERRUPT ROUTINE.
THE CAT11 EXECUTIVE PROGRAM CHANGES SLIGHTLY WITH INTERFACE USED, BUT ALL ROUTINES ARE IDENTICAL.

NEW***************	NEW ENTRY
READER SERVICE	REF 12.5023
CLASS CODE -	.543
TITLE- - - -	PRECOMPILER FOR IML SUBSET
AUTHOR(S)- -	W. KNEIS
PUBL. REF. -	CAMAC BULLETIN NO 10, JUNE 1974, AND GFK REPORT KFK2121, GFK, 1975 (IN PRESS)
NAME/ACRONYM -	META-II/X
OBTAINABLE FROM	W. KNEIS, IAK II/CYCLOTRON,GFK, D 7500 KARLSRUHE, POSTFACH 3640
AVAILABLE ON/AS	TAPE, CARDS
OPERATIVE DATE-	JULY 1974
COMPUTERS-	IBM/370 (TRANSL.), CDC 3100 (EXECUTION)
INTERFACE(S) -	IN-HOUSE TYPE
MIN MEMORY SPACE	36K BYTES (MAX 86K BYTES)
SOFTWARE TYPE -	PRECOMPILER (METACOMPILER SYSTEM)
LANGUAGES-	IML (USER), FORTRAN IV (SYSTEM), META-II (FOR COMPILER/WRITING)
INCORP TECHNIQUE	IN-LINE
HOST LANGUAGE -	COMPASS ASSEMBLER (CDC 3100)
FACILITIES -	SINGLE ACTIONS, MULTIPLE ACTION(MA) BLOCKTRANSFER(UBL), AND LAM-, CRATE-, AND SYSTEM-STATEMENTS

DESCRIPTION--
META-II/X IS A SYSTEM FOR WRITING COMPILERS. THE IMPLE-MENTED VERSION OF THE IML PRECOMPILER IS A CROSS-COMPILER VERSION, I.E. TRANSLATION IS DONE ON AN IBM/370, EXECUTION ON A CDC 3100 COMPUTER. THE OBJECT CODE FOR PRECOMPILING IS THE MNEMONIC COMPASS ASSEMBLER (CDC), THEREFORE AN ADDITIO-NAL ASSEMBLER STEP IS INVOLVED. WITH META-II/X A PRECOM-PILER CAN BE WRITTEN AND TESTED IN A FEW DAYS. THE IML SUB-SET CONTAINS THE DECLARATION- (LOCL, LOCD) AND ACTION-STATE-MENTS (SA, SJQ, SJNQ, MA, UBL, ALL LAM HANDLING-, SYSTEM- AND CRATE-CONTROLLRR- STATENENTS).
SET CONTAINS THE DECLARATION STATEMENTS LOCL AND LOCD. THE SUBSET ALSO CONTAIN ACTION STATEMENTS SUCH AS SA, SJQ, SJNQ, MA, UBL, ALL LAM-HANDLING STATEMENTS, SYSTEM STATEMENTS, AND CRATE CONTROLLER STATEMENTS.

```
READER SERVICE      REF 12.5024
CLASS CODE -        .544(BASIC)
TITLE- - - -        A PDP-11 BASIC EXTENSION FOR CAMAC
                    PROGRAMMING
AUTHOR(S)- -        I BALS, E DE AGOSTINO, CNEN, ROME
PUBL. REF. -        CAMAC BULLETIN NO 7, JULY 1973
OPERATIVE DATE-     1973
COMPUTER -          PDP-11
INTERFACE(S) -      EXECUTIVE SUITE (GEC ELLIOTT)
SOFTWARE TYPE -     INTERPRETER
INCORP TECHNIQUE    SUBROUTINES IN ASSEMBLY CODE
ENVIRONMENT FOR -   CAMAC SOFTWARE IS BASIC
LANGUAGE -          BASIC (EXTENDED)
```

```
DESCRIPTION- -
THE SUBROUTINES WHICH EXTEND THE BASIC INTERPRETER TO CAMAC
ARE CALLED BY AN EXTERNAL FUNCTION STATEMENT, WHERE ADDRESS,
FUNCTION, ETC, ARE TRANSMITTED AS ARGUMENTS. THE STATEMENT
HAS THE FOLLOWING GENERAL FORM- -
LET U = EXF (A1,A2, ...., ,A10)
THE FIRST ARGUMENT SELECTS THE APPROPRIATE SUBROUTINE.
DATALESS, READ, AND WRITE OPERATIONS WITH DIRECT/INDIRECT
ADDRESSING ARE POSSIBLE. ALSO SINGLE OR BLOCK TRANSFERS IN
ADDRESS SCAN, REPEAT OR STOP MODES CAN BE PERFORMED.
THE EXTENSION FEATURES LAM HANDLING.
```

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CORR**************  CORRECTED, REVISION A
READER SERVICE      REF 12.5025
CLASS CODE -        .544(BASIC)
TITLE- - - -        A CAMAC EXTENDED BASIC LANGUAGE
AUTHOR(S)- -        J M SERVENT (SCHLUMBERGER)
PUBL. REF. -        PROC CAMAC SYMPOS, LUXMBG, DEC 1973
NAME/ACRONYM -      CASIC
OBTAINABLE FROM     SCHLUMBERGER (SEE INDEX OF MFRS)
OPERATIVE DATE-     1973
COMPUTER -          PDP-11, 16K WORDS MEMORY
INTERFACE(S) -      ICP11 OR JCC11 (SCHLUMBERGER)
SOFTWARE TYPE -     INTERPRETIVE LANGUAGE, EXTENDED
                    WITH MACRO-INSTRUCTION GENERATOR
LANGUAGE -          BASIC (EXTENDED)
INCORP TECHNIQUE    IN-LINE CAMAC STATEMENTS
CAMAC FACILITIES    SYMBOLIC DEVICE NAMES, INTERRUPT
                    HANDLING, RE-ENTRANT.
```

```
DESCRIPTION- -
STANDARD BASIC IS EXTENDED WITH A SET OF CAMAC RELATED
STATEMENTS.  EXECUTION TIME FOR A 100 LINE PROGRAM IS ABOUT
10 SECONDS.  DECLARATIVE STATEMENTS ALLOW SYMBOLIC REFERENCE
OF A MODULE.  ADDRESS PARAMETERS CAN BE CONSTANTS
OR VARIABLES, EVEN EXPRESSIONS, THUS PROVIDING GREAT
FLEXIBILITY.  SEVERAL CONTROL FUNCTIONS ARE IN MACRO-STATE-
MENT FORM, SUCH AS - TST LAM MODULE (SAME AS MODULE(8)).
TYPICAL STATEMENTS--
ASSIGN ADDRESS - - ASSI MODULE = STA(B,C,N,A)
WRITE TO MODULE- - MODULE(F) = ARRAY(I)
READ FROM MODULE - ARRAY(I) = MODULE(F)
MODULE - MODULE- - MODULE1(16) = MODULE2(1)
CONTROL FUNCTION - EXEC MODULE(F)
LAM REG OPERATION- CLR LAM MODULE (=MODULE(10))
LAM/INTERRUPT- - - ON LAM(MODULE) DO 100
```

```
READER SERVICE      REF 12.5026
CLASS CODE -        .544(FOCAL)
TITLE- - - -        FOCAL OVERLAY FOR CAMAC DATA
                    AND COMMAND HANDLING
AUTHOR(S)- -        F MAY, H HALLING, K PETRECZEK
PUBL. REF. -        CAMAC BULLETIN NO 1, JUNE 1971
NAME/ACRONYM -      FOCADAT
OPERATIVE DATE-     1970
COMPUTER -          PDP-8, 4K OR 8K 12 BIT WORD MEMORY
INTERFACE(S) -      IN-HOUSE CC & INTERFACE
SOFTWARE TYPE -     INTERPRETER (EXTENDED)
INCORP TECHNIQUE    CAMAC EXTENSION OF OVERLAY,
                    IN-LINE CODING OF CAMAC COMMANDS
ENVIRONMENT FOR -   CAMAC SOFTWARE IS FOCAL
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DESCRIPTION- -
THE INTERPRETER IS PRIMARILY INTENDED FOR EASILY PROGRAMMED
ON-LINE CAMAC SYSTEMS IN NON-TIME-CRITICAL CONTROL AND DATA
HANDLING APPLICATIONS AND FOR TEST ROUTINES.
THERE ARE 9 CAMAC STATEMENT TYPES COVERING GENERAL CONTROLS
(Z, C. I) AND CAMAC COMMANDS WITH/WITHOUT DATA TRANSFER.
THE GENERAL FORM OF A CAMAC STATEMENT IS --
+A CF,C,N,A,F,FB,HW [,LW,Q]
WHERE SEVERAL PARAMETERS MAY BE OMITTED.
```

```
READER SERVICE      REF 12.5027
CLASS CODE -        .544(BASIC)
TITLE- - - -        8-USER BASIC UNDER DOS WITH
                    INTERPRETER EXTENDED FOR CAMAC
AUTHOR(S)- -        PFEIFFER, SPICKMAN, CARLEBACH
VERSION- - -        001
MAINTENANCE BY-     D P PFEIFFER
OBTAINABLE FROM     D P PFEIFFER, ZAM, KFA, JUELICH
AVAILABLE ON/AS     DECTAPE
OPERATIVE DATE-     JANUARY 1974
COMPUTER -          PDP-11, 16K OF 16 BIT WORD MEMORY
INTERFACE(S) -      TYPE 1533A (BORER)
MIN SYSTEM CONFIG   DOS V08 OR V09, 16K
SOFTWARE TYPE -     DOS SYSTEM INTERFACE TO CAMAC
LANGUAGE -          BASIC
INCORP TECHNIQUE    EXTENSION OF INTERPRETER
```

```
DESCRIPTION- -
THE 8-USER BASIC CAN BE RUN UNDER DOS. A HELP FILE CONTAINS
ALL MODIFICATIONS OF THE 1 TO 8 USER BASIC.  NO INTERRUPT
HANDLING.  COMMUNICATION BETWEEN THE 8 USERS IS POSSIBLE BY
ONE COMMUNICATION WORD PER USER.  EXPANDED ERROR MESSAGE
HANDLING.  FILE HANDLING EXTENDED.  TIME COMMAND ADDED.
```

```
READER SERVICE      REF 12.5028
CLASS CODE -        .544
TITLE- - - -        ORACL (TM), AN INTERPRETIVE REAL-
                    TIME MONITOR WITH CAMAC SUPPORT
AUTHOR(S)- -        L BYARS, R KEYSER (ORTEC INC)
NAME/ACRONYM -      ORACL (TM)
MAINTENANCE BY-     ORTEC
OBTAINABLE FROM     ORTEC (SEE INDEX OF MANUFACTURERS)
AVAILABLE ON/AS     PAPER TAPE AND DISK
OPERATIVE DATE-     APRIL 1974
COMPUTER -          PDP-11, MIN 5K 1L BIT MEMORY
INTERFACE(S) -      TYPE DC011 (EG&G)
MIN SYSTEM CONFIG   TTY & DC011
SOFTWARE TYPE -     INTREPRETER, SYSTEM MONITOR
LANGUAGE -          PDP-11 ASSEMBLER
INCORP TECHNIQUE    EMBEDDED CAMAC FEATURES
CAMAC FACILITIES    SINGLE OR MULTIPLE INSTRUCTIONS,
                    DEMAND HANDLING IS INCLUDED.
```

```
DESCRIPTION- -
ORACL INTERPRETS ARITHMETIC STATEMENTS, PROGRAM CONTROL
STATEMENTS, COMMENTS, I/O STATEMENTS, AND HARDWARE CONTROL
STATEMENTS AND EXECUTES THE DESIRED FUNCTION.

ORACL (TM) IS A TRADE MARK REGISTERED BY ORTEC, INC.
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.55 Support Software II

READER SERVICE	REF 12.5029
CLASS CODE =	.553(FOCAL/PAL)
TITLE= = = =	A FOCAL INTERRUPT HANDLER FOR CAMAC
AUTHOR(S)= =	F MAY, W MARSCHIK, H HALLING
PUBL. REF. =	CAMAC BULLETIN NO 6, MARCH 1973
NAME/ACRONYM =	FOCALINT
OPERATIVE DATE=	1971
COMPUTER =	PDP=8
SOFTWARE TYPE =	INTERRUPT HANDLER (SYSTEM PROGRAM)

DESCRIPTION= =
FOCALINT IS A GENERAL PURPOSE SYSTEM PROGRAM, ADAPTABLE FOR SPECIAL USE. UP TO 3 CRATES WITH 24 INTERRUPTS EACH CAN BE SERVICED. ONE PROGRAM LINE IN FOCAL IS RESERVED FOR EACH INTERRUPT. SHORT ROUTINES CAN BE TYPED INTO THESE LINES SERVICING THE ASSOCIATED INTERRUPTS, ALTERNATIVELY A FOCAL SUBROUTINE CAN BE USED. CURRENT LINE IN THE BACKGROUND PROGRAM WILL BE FINISHED BEFORE JUMPING TO INTERRUPT ROUTINE AND RETURNS TO NEXT LINE IN THE BACKGROUND PROGRAM AFTER SERVICING.

.57 Test Routines

NEW***************	NEW ENTRY
READER SERVICE	REF 12.5030
CLASS CODE =	.57
TITLE= = = =	TEST PROGRAMS FOR SYSTEMS, BRANCH DRIVER & MODULES
OBTAINABLE FROM	BI RA SYSTEMS (SEE INDEX OF MFRS)
OTHER REMARKS	FOR BRANCH DRIVER MBD=11, SYSTEM TEST MODULE 6102, AND DATA MODULES

DESCRIPTION==
A SET OF THREE DIAGNOSTIC PROGRAMS ARE SUPPLIED WITH THE MBD=11 MICROPROGRAMMED BRANCH DRIVER. TESTS OF MEMORY, FILE REGISTERS, INSTRUCTION SET, DMA TRANSFERS, INTERRUPTS ETC.
A COMPLETE SYSTEM TEST IS SUPPLIED WITH 6102.
A CAMAC TEST ROUTINE IS SUPPLIED FOR CAMAC MODULE TESTING FROM THE TELETYPE. NO ASSEMBLY LANGUAGE KNOWLEDGE REQUIRED.

READER SERVICE	REF 12.5031
CLASS CODE =	.573
TITLE= = = =	CAMAC TEST PROGRAM
AUTHOR(S)= =	DR. R MERTENS, IKP, KFA, JUELICH
AVAILABLE ON/AS	PAPER TAPE, ASCII CODE
OPERATIVE DATE=	1971
COMPUTER =	PDP=11, 16K OF 16 BIT WORDS MEMORY
INTERFACE(S) =	TYPE 2200 (BORER)
SOFTWARE TYPE =	TEST ROUTINES, STAND=ALONE PROGRAMS

DESCRIPTION= =
STAND ALONE PROGRAMS TEST SOME FUNCTIONS OF THE BORER TYPE 2200 INTERFACE, THE CRATE CONTROLLER AND TWO IN=HOUSE MODULES (C01 & C02).
ERROR MESSAGES ARE OUTPUT IF THERE ARE HARDWARE FAILURES.

READER SERVICE	REF 12.5032
CLASS CODE =	.573
TITLE= = = =	3911A TEST CAMAC
AUTHOR(S)= =	L A KLAISNER
OBTAINABLE FROM	KINETIC SYSTEMS (SEE INDEX OF MFRS)
OPERATIVE DATE=	1973
COMPUTER =	PDP=11, 4K OF CORE MEMORY REQUIRED
INTERFACE(S) =	TYPE 3911A (KINETIC)
SOFTWARE TYPE =	TEST ROUTINE

DESCRIPTION= =
A STAND ALONE PROGRAM FOR EXERCISING A CAMAC SYSTEM FROM A TELETYPE. IT SUPPORTS UP TO 8 CRATES WITH MODEL 3911A UNIBUS *) CRATE CONTROLLERS. A FUNCTION MAY BE EXECUTED ONCE OR REPETITIVELY.

*) UNIBUS IS A TRADE MARK OF DIGITAL EQUIPMENT CORP.

READER SERVICE	REF 12.5033
CLASS CODE =	.573
TITLE= = = =	TEST CAMAC
OBTAINABLE FROM	KINETIC SYSTEMS (SEE INDEX OF MFRS)
OPERATIVE DATE=	1972
INTERFACE(S) =	TYPE KS0011 (KINETIC)
COMPUTER =	PDP=11, 4K OF CORE REQUIRED
SOFTWARE TYPE =	TEST ROUTINE

DESCRIPTION= =
A STAND ALONE PROGRAM FOR EXERCISING A CAMAC SYSTEM FROM A TELETYPE. IT SUPPORTS ONE BRANCH DRIVER WITH UP TO 7 CRATES. A FUNCTION MAY BE EXECUTED ONCE OR REPETITIVELY.

READER SERVICE	REF 12.5034
CLASS CODE =	.573
TITLE= = = =	PDP=11 INTERFACE TEST PROGRAM
OBTAINABLE FROM	GEC=ELLIOTT (SEE INDEX OF MFRS)
OPERATIVE DATE=	1974
COMPUTER =	PDP=11
INTERFACE(S) =	PDP=11 EXECUTIVE SUITE/GEC=ELLIOTT
SOFTWARE TYPE =	TEST ROUTINE
LANGUAGE =	PAL=11 ASSEMBLER

DESCRIPTION= =
THIS IS A STAND=ALONE PROGRAM USED IN CHECKING THE EXECUTIVE SUITE, A MODULAR PDP=11 = CAMAC INTERFACE. DIAGNOSTIC MESSAGES ARE ISSUED.

NEWS

CAMAC AT COMPEC '74

The decision of the UK CAMAC Association to organise a major CAMAC event at COMPEC '74, the Computer Peripheral, Small Computers and Systems Exhibition and Conference held in London 26-28th November, proved to be an outstanding success. The Association took a large stand, and presented working CAMAC systems that attendees at the exhibition could get their hands on and drive, giving a powerful demonstration of the ease with which CAMAC I/0 systems can be handled.

The Association also played host to 10 companies involved with CAMAC namely:

— Applied Computer Systems Ltd. (ACSL)
— Computer Field Maintenance Ltd. (CFM)
— Dekon Electronic Systems Ltd.
— Logica Ltd.
— GEC Elliott Process Automation Ltd.
— Nuclear Enterprises Ltd.
— Semra-Benney (Electronics) Ltd.
— Grenson Electronics Ltd.
— Tekdata Ltd.
— Imhof-Bedco Ltd.

This showing of the extent of the commercial support for CAMAC, greatly added to the impact of the demonstrations. Borer Ltd. and GEC Elliott Process Automation Ltd. both had their own stands adjacent to the Association's stand forming a specially highlighted CAMAC section to the exhibition, while the Nuclear Enterprises Ltd. stand elsewhere in the exhibition hall served to further emphasise the total CAMAC impact.

Some 8 000 people visited the exhibition during the three days, and the volume of interest, often from people learning of CAMAC for the first time, was very great indeed.

COMPEC combines a specialist exhibition with conference sessions and a whole day was devoted to the presentation of papers on CAMAC. The session was organised by T. Peatfield, the UK CAMAC Association's Chairman, and the following papers were presented:

— CAMAC as a Systems Engineer's Tool, T. Peatfield, Daresbury Laboratory;
— Computer Communications and Data Networks, B. Zacharov, Daresbury Laboratory;
— CAMAC in Nuclear Physics and Medicine, J. Griffiths, Nuclear Enterprises Ltd.;
— A Review of CAMAC Software, F. Golding, ACS Ltd.;
— CAMAC in Process Control, K. Hilton, GEC Elliott Process Automation Ltd.;
— CAMAC in The Next Decade, H. Bisby, UKAEA Harwell.

As a direct result of its involvement with COMPEC, the UK CAMAC Association attracted a considerable volume of press coverage for its work and successfully expanded its membership. Anyone wishing to have more information about the Association (see p. 12 of this issue) should contact the Secretary:

Mr. R. North,
UK CAMAC Association,
c/o Department of Medical Electronics,
St. Bartholomew's Hospital
London E.C. 1

NEWS

ANNOUNCEMENTS BY CAMAC MANUFACTURERS

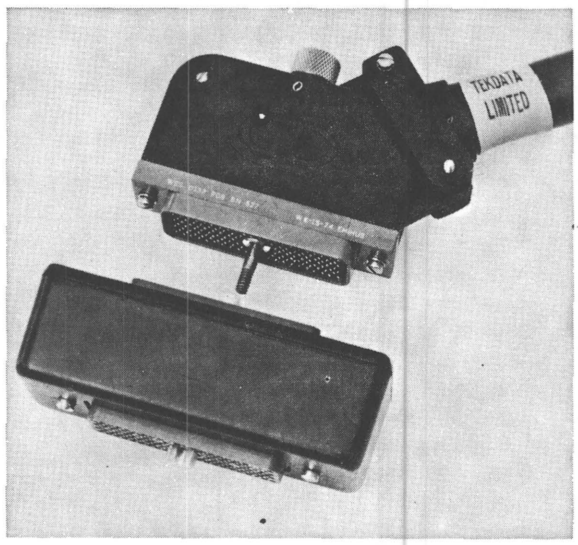
TEKDATA LIMITED offer a Branch Highway Harness Junction Box as the latest item in their range of CAMAC interconnection products.

The junction box is designed specifically to interconnect the standard 132 way plugs. However, it has also been designed for the 108 way, 88 way, 56 way and 38 way EMIHUS connectors. Many other types of connectors can also be accomodated including the Cannon 'D' type range.

One major advantage of the product is its compactness. The size is 88 mm × 35 mm × 30 mm deep. The pins are interconnected by the same gauge of twisted pair wire that is used on Tekdata's range of Branch Highway harnesses.

When ordening, quote the part no. 5849 and specify the type of connector to be used.

Ref. No. 12.0001



HOW TO CONTACT CAMAC WORKING GROUPS

Everybody who is interested in further information on the activities of the CAMAC Working Groups or who would like to obtain advice for the application of CAMAC specifications is invited to contact the appropriate chairman or secretary of the existing working groups. The corresponding addresses are given below.

ESONE-CAMAC WORKING GROUPS

Dataway Working Group (EDWG)

Chairman: R. Patzelt, Technische Hochschule Wien, 1040 - Wien, Gusshausstr. 21, Austria.

Secretaries: R.C.M. Barnes and I.N. Hooton, both of Electronics and Applied Physics Div., Building 347.2, AERE Harwell, Didcot, Oxfordshire OX11ORA, England.

Software Working Group (ESWG)

Chairman: I.N. Hooton, see above.

Secretary: A. Lewis, Electronics and Applied Physics Div., AERE Harwell, Didcot, Oxfordshire OX11ORA England.

Analogue Signals Working Group (EAWG)

Chairman: Th. Friese, Hahn-Meitner-Institut für Kernforschung Berlin GmbH, 1 Berlin 39, Glienickerstr. 100, Germany.

Mechanics Working Group (EMWG)

Chairman: F.H. Hale, Electronics and Applied Physics Div., Building 347.2, AERE Harwell, Didcot, Oxfordshire OX11ORA, England.

Information Working Group (EIWG)

Chairman: H. Meyer, CBNM EURATOM, Steenweg naar Retie, 2440 Geel, Belgium.

NIM-CAMAC WORKING GROUPS

Dataway Working Group (NDWG)

Chairman: F.A. Kirsten, Lawrence Berkeley Laboratory, University of California, Berkeley, Cal. 94720, U.S.A.

Secretary: R.J. Martin, FNAL, P.O. Box 500, Batavia, Illinois 60510, U.S.A.

Serial Systems Sub-group

Chairman: D.R. Machen, Los Alamos Scientific Laboratory, University of California, LAMPF/MP-1, Los Alamos, New Mexico 87544, U.S.A.

Block Transfers Sub-group (joint with NSWG)

Chairman: E.J. Barsotti, FNAL, P.O. Box 500, Batavia, Illinois 60510, U.S.A.

Systems Compatibility Sub-group

Chairman: D. Horelick, Stanford Linear Accelerator Center, Stanford University, P.O. Box 4349, Stanford, California 94305, U.S.A.

Software Working Group (NSWG)

Chairman: R.F. Thomas, Jr., Los Alamos Scientific Laboratory, Los Alamos, New Mexico 87544, U.S.A.

Secretary: W.K. Dawson, University of Alberta, Dept. of Physics, Edmonton, Alberta, Canada.

Mechanical and Power Supplies Working Group (NMWG)

Chairman: L.J. Wagner, Lawrence Berkeley Laboratory, University of California, Berkeley, California 94720, U.S.A.

Analogue Signals Working Group (NAWG)

Chairman: D.I. Porat, Stanford Linear Accelerator Center, Stanford University, P.O. Box 4349, Stanford, California 94305, U.S.A.

MEMBERSHIP OF THE ESONE COMMITTEE

This list shows the member organisations and their nominated representatives on the ESONE Committee. Members of the Executive Group are indicated thus*.

International	European Organization for Nuclear Research (CERN)	*F. Iselin**	Genève, Suisse
	Centro Comune di Ricerca (EURATOM)	*L. Stanchi*	Ispra, Italia
	Bureau Central de Mesures Nucléaires (EURATOM)	*H. Meyer**	Geel, Belgique
	Institut Max von Laue - Paul Langevin	*NN*	Grenoble, France
	Joint Institute for Nuclear Research	*B.V. Fefilov*	Dubna, USSR
Austria	Studiengesellschaft für Atomenergie	*W. Attwenger*	Wien
	Inst. für Elektrotechnische Messtechnik an der T.H.	*R. Patzelt*	Wien
Belgium	Centre d'Etude de l'Energie Nucléaire	*L. Binard*	Mol
Denmark	Forsögsanläg Risö	*P. Skaarup*	Roskilde
England	Atomic Energy Research Establishment	*H. Bisby*	Harwell
	Culham Laboratory	*A.J. Vickers*	Abingdon
	Daresbury Nuclear Physics Laboratory	*A.C. Peatfield**	Warrington
	Rutherford High Energy Laboratory	*M.J. Cawthraw*	Chilton
	University of Oxford	*R. Hunt*	Oxford
	University of York	*I.C. Pyle*	Heslington
Finland	Institute of Radiation Physics	*B. Bjarland*	Helsinki
France	Centre d'Etudes Nucléaires de Saclay	*P. Gallice**	Gif-sur-Yvette
	Centre d'Edutes Nucléaires de Grenoble	*J. Lecomte*	Grenoble
	Laboratoire de l'Accélérateur Linéaire		Orsay
	Centre de Recherches Nucléaires	*G. Metzger*	Strasbourg
	Laboratoire d'Electronique et d'Instrumentation Nucléaire du Centre Universitaire du Haut Rhin	"	Mulhouse
	Laboratoire des Applications Electroniques de l'Ecole d'Ingénieurs Physiciens	"	Strasbourg
F.R. Germany	Deutsche Studiengruppe für Nukleare Elektronik c/o Physikalisches Institut der Universität	*B.A. Brandt*	Marburg
	Deutsches Elektronen-Synchrotron	*H.-J. Stuckenberg*	Hamburg
	Hahn-Meitner-Institut für Kernforschung	*K. Zander**	Berlin
	Kernforschungsanlage Jülich	*K.D. Müller*	Jülich
	Gesellschaft für Kernforschung	*J.G. Ottes*	Karlsruhe
	Institut für Kernphysik der Universität	*W. Kessel*	Frankfurt/Main
	Max-Planck-Institut für Plasmaphysik	*D. Zimmermann*	Garching
Greece	Demokritus' Nuclear Research Centre	*Ch. Mantakas*	Athens
Hungary	Central Research Institute for Physics	*J. Biri*	Budapest
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	CNEN Laboratori Nazionali	*M. Coli*	Frascati
	CNEN Centro Studi Nucleari	*F. Fioroni*	Casaccia
	Centro Studi Nucleari Enrico Fermi	*P.F. Manfredi*	Milano
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Switzerland	Schweizerische Koordinationstelle für die Zusammenarbeit auf dem Gebiet der Elektronik	*H.R. Hidber*	Basel
Yugoslavia	Boris Kidrič Institute of Nuclear Sciences	*M. Vojinovic*	Vinča Belgrade
Affiliated Laboratories			
Canada	TRIUMF Project, University of British Columbia Simon Fraser University, University of Victoria, University of Alberta	*W.K. Dawson*	Edmonton
German Dem. Rep.	Akademie der Wissenschaften	*J. Lingertat*	Berlin

LIAISON WITH THE U.S. AEC NIM COMMITTEE IS MAINTAINED THROUGH:

L. Costrell (Chairman) National Bureau of Standards – Washington, DC.

4

CAMAC MODULES FOR INDUSTRIAL ANALOG MEASUREMENT EQUIPMENT

by

J. Biri, L. Somlai, Gy. Somogyi

Central Research Institute for Physics, Budapest, Hungary

Received 12th November 1974

SUMMARY A family of CAMAC modules for analog measurements has been developed as the first step towards meeting the requirements of industrial applications.

In recent years there has been more and more demand for industrial use of CAMAC. Some major firms have investigated the use of CAMAC[1], and have shown that the CAMAC system is good for these new applications. Two problems were still to be solved: the mechanical construction, shielding and grounding has to meet industrial standards; and an appropriate family of special industrial modules have to be designed.

To meet these needs we designed an industrial analog measuring system. This is only the first step towards industrial type module families: analog outputs, digital in- and output systems have to be designed too.

DESIGN PRINCIPLES

The main design principles were the following:

- The system should be protected against electrical noise.
- The inputs should be decoupled from the computer system, so that the system is intrinsically safe.
- The connectors and cables should meet industrial standards.
- Speed is not critical, the measurements are generally rather slow.
- The family of modules should be complete: it should contain power supplies, bridges, etc., besides multiplexers and ADC's.

NOISE PROTECTION

The requirement of noise protection is fulfilled as follows. Every module, even the bridge power supplies, has guarded shielding, and the A/D converter has a floating input. The A/D converter has high common-mode rejection (120dB at 50Hz) and series mode rejection too. In the multiplexer, every input can have a specific matching or terminating circuit, which can be placed on small boards individually. The A/D converter is an integrating type.

The cables carrying the analog signals have three or four twisted wires and are shielded. Their size is bigger than the usual cables used in laboratories, therefore we had to use special connectors too: these are the AMP 201 356-3 and 925 173-2 types.

FAMILY OF MODULES

The family of our analog measuring equipment consists of the following modules, shown in Figs. 1 and 2. The *analog to digital converter* is a floating-input, integrating type converter based on the

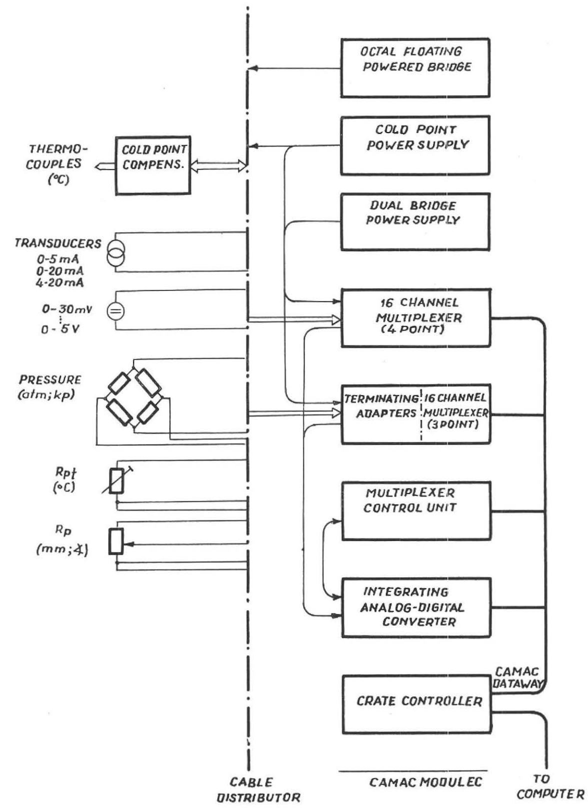

Fig. 1 Industrial analog Module Family (schematic)

amplitude-frequency conversion principle where integration is achieved digitally by an up-down counter. Voltage range and integrating time can be changed by program.

There are two types of *multiplexers* in the system: the first switches three contacts per channel (high, low, guard), the other switches four. One module switches 16 channels, but all the multiplexer modules in a crate can be connected together by chaining. Every channel has a small card, where either a bridge or a filter or some special circuit can match the multiplexer to the measured channel. There is also a common group relay which can disconnect the common output. The four-point-per-channel multiplexer can switch not only the input analog signal, but also a bridge or power supply, which feeds the sensors. A *multiplexer control unit* serves to control both types of multiplexers.

The following modules have no connection to the Dataway, but are placed in CAMAC module mechanics.

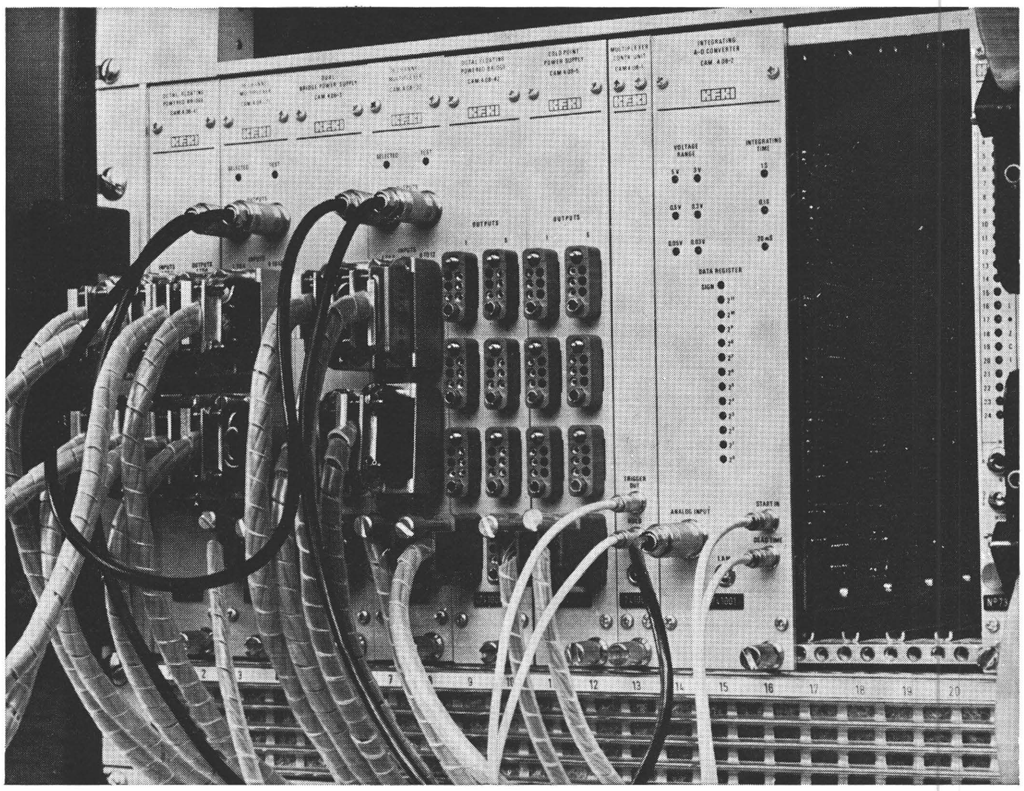

Fig. 2 Some Modules from the Family

A *Bridge Power Supply module* can feed bridges or external devices. By internal patch connection it can be either a voltage or a current generator. In one module there are two supplies. The supplies are guarded, have floating outputs, and are isolated from the mains; they use DC-DC converters.

Two types of *bridge modules* are primarily for Pt-thermo-resistors: the first type can be used with the three-point, the other with the four-point multiplexer. The bridge modules have their own floating power supplies. There are 8 bridges in a module.

Cold point compensators and their power supply complete the family. The cold point compensators are not in CAMAC mechanics, but in heavy boxes, to be placed near the thermocouples. All the power supplies and bridges are also guarded, so the whole system is continuously guarded from the sensing element to the A/D converter.

APPLYING THE FAMILY OF MODULES

In the following we show various examples for different sensing elements or inputs. Fig. 3a shows the simplest connection: a transducer or voltage supply is connected through the 3-point multiplexer

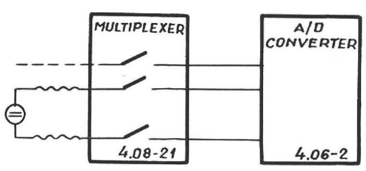

Fig. 3a) Simplest Configuration: 3 Point Multiplexer and A/D Converter

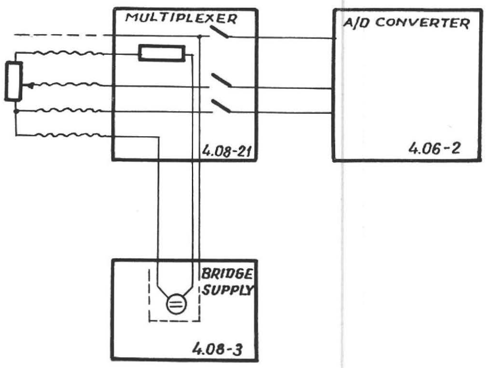

Fig. 3b) Use of the Bridge Supply

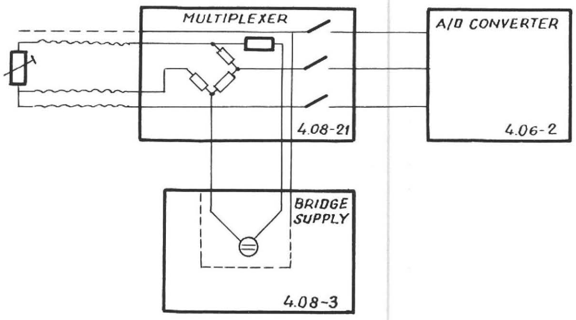

Fig. 3c) The individual Matching Circuit of the Multiplexer contains a Bridge

to the A/D converter. Figs. 3b and 3c show the use of a bridge supply: in both cases the multiplexer is the same. In the first case the individual matching circuit on the small card is a simple resistor, while in the second case it is a bridge. The use of a 4-point multiplexer is shown in Fig. 3d. The bridge can be common to a whole group of variable resistors.

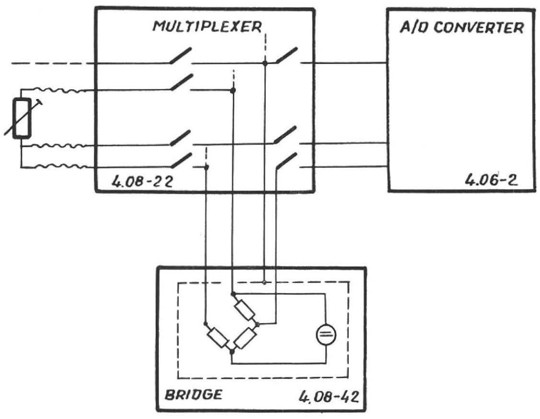

Fig. 3d) The common Bridge in a separate Module; Use of the 4 Point Multiplexer

When this group is not selected, the group relay disconnects the whole set of inputs from the A/D converter.

OTHER ACTIVITIES

The design of this analog module family is only the first step towards our industrial CAMAC applications. We are working in four fields to broaden industrial use of CAMAC:

- In the software field we have worked out drivers to handle our industrial system in a higher level language.
- We have started work on industrial analog output systems:
- New modules are being designed for the analog input system too, e.g. flying capacitor multiplexers.
- We are getting experience with our new family of modules in various application fields, such as power stations and melting ovens.

REFERENCE

1. Lyon, W.T., An Evaluation of CAMAC Equipment in an Industrial Environment. Proceedings of the First International Symposium on CAMAC in Real-Time Computer Applications, *Supplement to CAMAC Bulletin*, Issue 9 (April 1974), p. 211.

5

A FAST MULTI-EVENT TIME-DIGITISER

by

J.P. Argyle, P.E. Dolley and G. Huxtable

Nuclear Physics Division, AERE Harwell, England

Received 9th September 1974

SUMMARY This time-digitiser, primarily for neutron time-of-flight measurements, is a 5-width CAMAC module. It measures the time intervals between a start pulse and a succession of event pulses with a resolution of 1.25 nsec and dead time of 110 nsec. It includes an 18-word data buffer.

Harwell has recently developed a time-digitiser in the CAMAC format, designed primarily for neutron time-of-flight measurements, though other applications are likely. This new digitiser complements the system recently described by Boyce and Morris[1], being suited to the shorter burst width (5nsec) and high instantaneous pulse rates of the Harwell Synchrocyclotron.

The new unit, a 5-width module, measures the times between a start pulse and a succession of event pulses in binary digital form. The digitised times are held in an 18-word buffer store, from which they can be read out onto the CAMAC Dataway. The basic time reference is a 100MHz free-running crystal clock. The resulting 10nsec time channels would be too wide for the required resolution, so an interpolation system has been incorporated. This measures and records the interval between each event pulse (or start pulse) and the succeeding clock, using a tapped delay line. The taps are spaced at 1.25nsec intervals, which determines the overall resolution of the system. The least significant bits of the time difference between start and event are obtained by subtracting the corresponding interpolator values by hardware before the digitised time goes to the buffer store.

The delay-line method of interpolation was chosen because of its high speed, as it was important to minimise the dead time between event inputs. After acceptance of an event, the sequence of digitising and subsequent transfer to the buffer store is complete within 110nsec, and the next event can then be accepted.

Because the start and event pulses occur at random times with respect to the clock, small errors in setting up the tapped delay line are largely cancelled out by the averaging process that takes place in the interpolator[2]. The small errors in channel-width that remain are cyclic variations repeating every 8 channels, the width of a channel deviating by no more than 1% from its nominal value of 1.25nsec.

The hardware registers can hold up to 18 events, but the system can accept an unlimited number of events if CAMAC Dataway cycles can keep unloading the buffer store to prevent it becoming full. The store is a circular buffer with independent load and unload pointers, operating on a first-in, first-out basis, and an output transfer can take place from the store without interrupting its availability for storing digitised events.

In each Dataway read operation 24 bits are transferred, of which up to 20 are time bits. This allows over a million channels of 1.25nsec width, giving an overall a timing range of 1.3msec. The remaining bits can be used as flags to transfer extra parameters describing the events.

The fast circuitry of the digitiser uses ECL 10 000 series logic, interfacing to TTL levels for the CAMAC control and data-transfer functions. The prototype, a hand-wired unit, has been used successfully for neutron data collection since October 1973. This first digitiser was designed and built within Nuclear Physics Division and a printed circuit version is now being developed in collaboration with Electronics Division at Harwell.

REFERENCES

1. Boyce, D.A., Morris, D.V., A CAMAC Time-of-Flight Scaler, *CAMAC Bulletin*, No. 8, March 1974, p. 9.
2. Cottini, *et al.*, Proc. Int. Conf. on Instrumentation for High Energy Physics, 1966, p. 171.

6

X-INTERRUPT CAMAC MODULE FOR USE WITH BORER 1533A CRATE CONTROLLER

by

I. Török

Joint Research Center, Ispra, Italy

(on leave from the Institute of Nuclear Research of the Hungarian Academy of Sciences, Debrecen, Hungary)

Received 3rd October 1974

SUMMARY A module has been developed to provide interrupts from both X and Q in systems with the Borer Type 1533A crate controller (used with PDP-11 computers).

The Borer Type 1533A dedicated crate controller for the PDP-11 computer can generate an interrupt when one of the Dataway responses Q X occurs. As supplied, it is wired to interrupt when Q occurs. With a very small modification in the controller, and using an additional single width CAMAC module, it is possible to have both interrupt types. Of course a free station is needed for this purpose in the crate. The XIR-1 is a module specially designed for this purpose.

The crate controller Type 1533A handles LAM interrupts and the Q interrupt in a similar way. All interrupt signals are inputs to a vector address generator. The last address (which has the lowest priority in the vector address generator) is used for the Q interrupt. The XIR-1 module takes the internal, prehandled X signal from the controller and sends it back as a normal LAM signal, using one of the interrupt vector addresses.

In the crate controller itself the only modification needed is to lead a wire from the internal X point to a Dataway connector P patch point. (In our case it was P5 at N = 24). In the Dataway of the crate one has to lead a wire from this P point to the P5 point of the station where the XIR-1 module will be used.

Fig. 1 is a block diagram of the module, which uses 10 integrated circuits. The X signal, pre-handled in the crate controller, enters the module through the P5 patch point of the Dataway connector. With a small delay after S1, the prehandled X signal is clocked into a D flip-flop which acts as the LAM status flip-flop. This flip-flop memorizes any X failure until it is cleared by a computer command. Another D flip-flop is the LAM mask flip-flop. When this mask permits, and the module is not addressed, the L signal is generated, to request an interrupt.

The module is cleared by (C+Z). S2, and performs the following CAMAC commands: F(8) (Test LAM), F(10) (Clear LAM), F(24) (Disable LAM), F(26) (Enable LAM), F(27) (Test LAM Status). On all the five functions the module gives

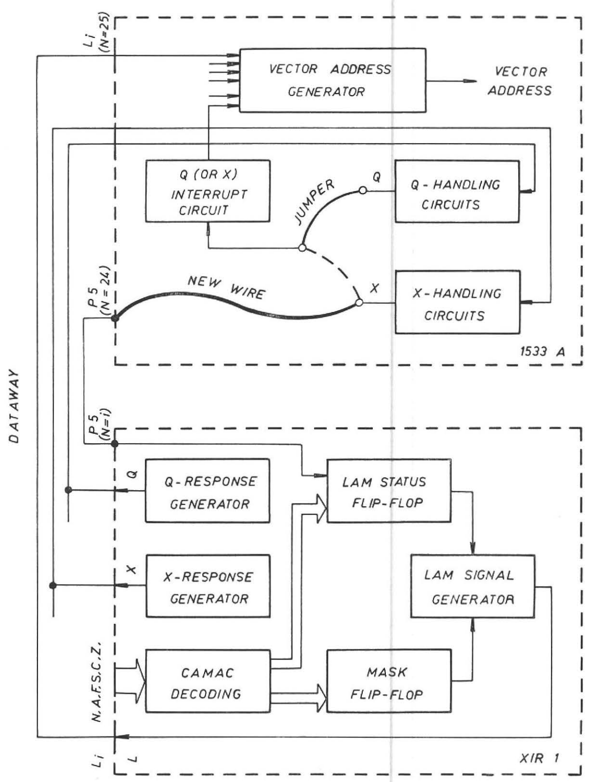

Fig. 1 Block Diagram of X-Interrupt Handling

the Dataway signal X = 1. The three non-test functions always give Q = 1. The two test functions give Q depending on the state of the flip-flops. Front panel lamps indicate the state of mask flip-flop and the LAM Status flip-flop.

Using this module for handling X interrupts is perhaps a little slower than using the internal interrupt logic in the controller, but this is already occupied by the Q interrupt handling. In practice the Q interrupt occurs much more frequently than the X interrupt, which is a warning of a serious malfunction. The XIR-1 module generates an interrupt with the same speed as the Q interrupt circuitry of the 1533A, but the resetting, masking and testing processes are a little longer, because they need a Dataway CAMAC cycle.

SOFTWARE

1

CAMAC EXTENSION FOR BASIC 2/3 ON THE ALPHA-LSI COMPUTER

by

J.L. Visschers and A. ten Hertog

Institute for Nuclear Physics Research, Amsterdam, The Netherlands

Received 25th October 1974

SUMMARY The BASIC software package for the ALPHA-LSI minicomputer is extended with CAMAC statements. This implementation allows real-time interrupts and is useful for module testing and slow process-control purposes.

INTRODUCTION

The new 300 MeV linear electron accelerator[1] at IKO will be controlled by a minicomputer network of 16 ALPHA-LSI processors. Each processor will, in addition to a fast DMA-type interface for pulse-to-pulse control, be equipped with a CAMAC crate for the connection of various slower signals both analog and digital.

In this application, we are planning to use a CAMAC-extended version of BASIC for several purposes, from simple testing of a single erroneous or own-developed CAMAC module to whole subsystem checkout during accelerator maintenance. The latter application needs real-time LAM treatment, which is discussed later in this paper.

THE CAMAC SINGLE-ACTION

The BASIC 2/3 implemented on our ALPHA-LSI computers[3] contains the CALL statement in the following form:

CALL (k, arg's)

where k is an integer, defining which machine-language coded subroutine is to be entered. The number of arguments passed to or from this subroutine is arbitrary, and is not even fixed for a given k. This BASIC implementation is thus of the middle level, according to the classification of I.C. Pyle[2].

The general CAMAC single-action needs the following arguments:

B – branch number
C – crate number within branch B
N — module number within C
A — subaddress within N
F — function to be performed (e.g. read or write)
D — data to be transferred (if any).

In our case, where we deal with a small single-crate system with severe core-limitations, we will abandon the parameters B and C, as they would be equal to 1 all the time. This leaves us with N, A and F to define the action, and D when the action is of the data-transfer type. To remain consistent with Pyle's proposals, it would now be necessary to have a separate module-select statement—e.g. CALL (1, N)—and an action statement—e.g. CALL (2, A, F) or CALL (2, A, F, D).

By automatic translation our future programs then could conform to the proposed standard-replacing "CALL (1," by "CALL (1, 1, 1,". This, however, has some disadvantages, which we will point out, in the real-time case. The difference between the proposed read and write operations becomes obsolete too, as there is no possibility of assigning a value to a CALL in our implementation. We therefore decided to have a CAMAC single-action subroutine which has the following two forms of calling:

CALL (1, N, A, F)	for a single action without data transfer (e.g. enable or disable)
CALL (1, N, A, F, D)	for read or write actions with data transferred to or from BASIC variable D.

Applying Ockham's razor again, we will introduce no special language elements for Clear, Zero, Inhibit, etc., but use only the explicit forms according to the Type A crate controller conventions:

CALL (1, 28, 8, 26)	: Zero (Initialise)
CALL (1, 28, 9, 26)	: Clear
CALL (1, 30, 9, 26)	: set Inhibit
CALL (1, 30, 10, 26)	: enable branch demand
CALL (1, 30, 0, 0, G1)	: read Graded-L pattern into the variable G1

A consideration is that statements of this category tend to occur sparsely in application programs.

Example: Continuous 24-bit I/O module test

```
 10  CALL (1, 28, 8, 26)
 20  R = Ø
 30  W = 16
 35  DIM B(24)
 40  FOR I = Ø TO 23
 50  B(I) = 2 ↑ I
 60  NEXT I
 70  PRINT "24-BIT I/O TEST"
 80  PRINT "TYPE MODULE POSITION"
 90  INPUT M
100  PRINT "TYPE SUBADDRESS"
110  INPUT A
120  FOR J = Ø TO 23
130  CALL (1, M, A, W, B(J))
140  CALL (1, M, A, R, C)
150  IF C = B(J) THEN 170
160  PRINT "BIT", J, "IS DEFECT"
170  NEXT J
180  GOTO 120
200  END
```

Q AND X SIGNALS

Each CAMAC single-action sets the status flip-flop's for Q and X. Q is generally used to read out the status of one-bit entities like LAM-bits, while X is only used to indicate whether the module was able to execute the required action. So, with a well-debugged program and error-free hardware, the $X = 0$ condition should never occur. It would therefore be wise to generate an error-exit and end the BASIC execution mode on detection of this condition. However, as the system will sometimes be used to test erroneous modules, the testing of X will be left to the application programmer's responsibility, by means of

CALL (2, Q, X) delivers the most recent Q and X values in the BASIC variables Q and X.

LAM TREATMENT IN REAL-TIME ENVIRONMENT

LAM signals occurring in real-time (i.e. not expected by the currently running thread of the program) have to be treated like interrupts in an assembly-code language. This means that the current execution of BASIC statements has to be interrupted and resumed after execution of a LAM-service routine, which will take care of the LAM, including resetting the LAM source.

We are implementing the following general scheme:

In the main program a CALL (1, 30, 1Ø, 26) has been executed previously to enable demands. Upon occurrence of a Branch Demand the branch-demand disable is executed immediately within the BASIC 2/3 interrupt service routine. A flag is set to indicate this and main-program execution is resumed until some apt point, e.g. the end of a BASIC statement, where the main program is interruptable. At that point in time, a GOSUB statement is simulated to a BASIC text-line number, which is predefined for each module-number. In our case we chose this number to be $99000 + 10*N$, where N is the lowest module-number among those occurring in the Graded LAM request. So if, for example, modules $N = 10$ and $N = 15$ simultaneously cause LAM's, the main program will be interrupted and execution will be resumed at line 99100 with branch-demands disabled. There the application programmer can service the LAM demand and finish his piece of program with a RETURN statement. This RETURN, corresponding to the simulated GOSUB, has the effect of resuming the main program execution with branch-demands enabled. In our example, the LAM of module 15 will then immediately be detected and a GOSUB 99150 is simulated, while the main program is still in interrupted state, and the branch-demand will be disabled again.

Thus, we have a more or less general scheme to treat real-time LAM's. The different modules have a fixed priority, depending on their position in the crate, and LAM-service routines will not be interrupted.

SOME REMARKS

- In the case of very time-consuming LAM-treatment it is of course possible to issue a CALL (1, 30, 10, 26) in the LAM-service routine, thus enabling other modules to have their LAM's served. But then it is advisable to first disable the LAM of the currently served module, to avoid stack-overflow condition in the BASIC interpreter. (This happens otherwise if the LAM of the module is repeated faster than its service-routine can execute).
- It will be clear that a module-select statement, like that considered under single-actions, will cause extra difficulties, as the currently selected module-number of the main program will have to be placed on the stack and restored after LAM treatment.
- If no LAM service routine is present, an error-exit specifying 'non existent line number' will be generated when the corresponding LAM is acknowledged.

OTHER USEFUL FUNCTIONS

When manipulating bits and registers in BASIC, some boolean operations (which of course can be performed by calculating in terms of powers of 2) are often used.

CALL (3, A, B, C) performs the logical AND between the (assumed) 24-bit integers A and B and stores the result in C

CALL (4, A, B, C) similar for logical OR

CALL (5, A, B, C) similar for logical XOR

The XOR is especially useful to compare two 24-bit patterns (e.g. a status register and its expected value) and obtain their differences:

$$XOR(2 \uparrow I, 2 \uparrow J) = 2 \uparrow I + 2 \uparrow J \text{ if } I \neq J < 24$$

Use of these machine-coded functions results in a considerable gain in execution speed.

ACKNOWLEDGEMENTS

This work is part of the research programme of the Institute for Nuclear Physics Research (I.K.O.) made possible by financial support from the Foundation for Fundamental Research on Matter (F.O.M.) and the Netherlands Organisation for the Advancement of Pure Research (Z.W.O.).

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2

CAMAC SOFTWARE-DRIVER FOR REAL-TIME SYSTEM RSX-11D ON THE PDP-11/40 OR 11/45

by

H. Heer and H. Pohl

Zentrallabor für Elektronik, KFA, Jülich, Germany

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SUMMARY A CAMAC software-driver for the Crate Controller Type 1533A (Borer Electronics) has been developed as an I/O-request-queue managing device-driver in the event-driven RSX-11 D real-time system.

THE SOFTWARE ENVIRONMENT

Unlike DOS-11, which can be used on any PDP-11, RSX-11 D relies heavily on the real-time and multi-programming facilities of the PDP-11/40 and 11/45, derived from two different machine features: special instructions, and a memory management unit capable of addressing 124k of memory and an additional 4k of device addresses (the external page).

The memory protection scheme using virtual 16-bit addresses also provides hardware protection for the real-time executive and the several user tasks that are in memory at the same time. Consequently, a normal user task is unable to access hardware device addresses (the external page) as well as the usual PDP-11 interrupt vector space at locations 0 to 1000 octal.

THE HARDWARE

In small CAMAC systems using one or two crates the Borer Crate Controller occupies the address space which is provided for user-supplied hardware in the external page. The LAM's of a crate can generate 16 different adjacent interrupt vectors whose base address is chosen by jumpers. These vectors normally point to addresses 0 to 1000 (octal).

THE RSX-11 D I/O CONCEPT

An I/O request from a task is implemented by issuing a system directive to queue a request for a logical unit number (LUN). The RSX-11 D executive puts the I/O request into a priority ordered queue for the device driver that serves the physical unit assigned to the LUN. Control is returned immediately to the user task. I/O completion is signalled in three possible ways:

- a significant event is declared and the event flag is set, as specified earlier by the user task at request time;
- indicators are set in an I/O status block within the requesting task;
- a program interrupt (asynchronous system trap) is performed for the requesting task.

THE CAMAC DRIVER

Loading the handler task by operator command causes execution of the initialisation part of the handler. It sets the 'resident bit' in the physical unit directory (PUD). By use of a system-supplied 'intermediate node' it connects any interrupt vector of the two crates to a handler routine for 'undefined interrupts'. The base address for these interrupt vectors is taken from an entry in the PUD, which is set up by a directive at system generation time. Any 'undefined interrupt' occurring after this point will generate a message at the operator console, listing crate and LAM numbers.

After initialisation the handler enters an 'idle' state, waiting for any event to occur.

This can be:

- a request from a task for a read, write or dataless CAMAC cycle;
- a connection to a LAM request;
- a disconnection from a LAM request;
- a termination of all I/O requests for a task which is going to exit;
- a termination of all CAMAC I/O because of the handler itself being unloaded by operator command.

Read and write requests are 24-bit transfers. In addition to supplying the normal RSX-11 D conventions (directive status word, I/O status word, user defined event flag and asynchronous system trap) the control and status register of the Crate Controller is read out and written to a user-supplied address, thus also giving Q and X information.

The Connect-to-LAM request deletes the entry for the undefined interrupt message of the specified LAM. The user gives the number of an event flag which has to be raised in the requesting task if the LAM occurs. The user also defines a CAMAC operation, which the handler stores in a special entry to be executed at interrupt time. Usually this operation will disable the LAM in the requesting station. By this method a very fast interrupt reaction time is achieved, because the validity checking process can be taken out of the interrupt handling and be done earlier at the dequeuing time of the request.

In a similar way the Disconnect-from-LAM request changes the special interrupt entry back to a jump to the 'undefined interrupt' handler.

From the request-dequeuing point to the execution of the CAMAC operation (which may be only two MOVE-instructions for 24-bit data) many system subroutines are used to provide the security and full protection of the RSX-11 D executive. This naturally slows down the handler's execution speed to typically 700 transfers/second for normal 24-bit Read or Write.

The flush-a-task's I/O or flush-all-I/O requests are handled as specified in RSX-11 D, entries in the queue or the queue itself are deleted and all interrupts are linked to the system's 'undefined interrupt' handling routine.

A CAMAC operation is requested by the normal RSX-11 D I/O request macro 'QIO' (i.e. put an Input-Output request in a priority-ordered Queue).

QIO fnc, lun, efn, pri, iost, ast, ⟨prmlst⟩
fnc = function code

WRITE	=	400 (WRITE CAMAC WORD)
READ	=	1000 (READ CAMAC WORD)
CTRL	=	1400 (CONTROL WORD)
CON	=	2000 (CONNECT INTERRUPT)
DISCO	=	2400 (DISCONNECT INTERRUPT)

lun = logical unit number e.g. 1
efn = event flag number e.g. 1
pri = priority
iost = Entry of the I/O — Status block in the user task
ast = Entry of the I/O DONE Asynchronous System Trap
⟨prmlst⟩ = CAMAC parameter list (P1, ..., P6)

The specific parameters for CAMAC I/O are:

P1: Module address defined in the user task e.g. D1 = 164040
P2: CAMAC function
P3: Data buffer in the user task.

FUTURE PLANS

During the development and writing of test programs for the CAMAC-driver, it appeared that the RSX-11 D I/O request scheme (using up to twelve parameters, a directive status word, and an I/O status block) was inconvenient for a more problem-oriented programmer. So there is a need for a higher level structure or language built up on the basic QIO-macros, e.g. calls from FORTRAN.

ACKNOWLEDGEMENT

We would like to thank Dr. Müller, Dr. Halling and Dr. Zwoll (KFA Jülich) for their advice and the DEC Special System's Group Munich for special hints concerning the device handler scheme of RSX-11 D.

NEWS

ANNOUNCEMENT BY CAMAC MANUFACTURERS

NUMELEC SA offers a new system controller for the connection of CAMAC crates to the computer series T-1600 of Télémécanique. The Type JCT-16-10 is a double-width unit for program-me-mode transfers (16-bits). For transfer in Direct Memory Acces mode (DMA) an additional double-width unit, Type JDM-16-10, is available. Extensions can be made to control up to as many as eight CAMAC crates in series.

Ref. no. 12.0002

BORER ELECTRONICS AG report that the sixth fully automatic warehouse under complete CAMAC control has just gone into operation. All the CAMAC equipment was supplied by the BORER company including display devices. Considerable adaption of the whole system was undertaken to meet the stringent requirements of a severe industrial requirement.

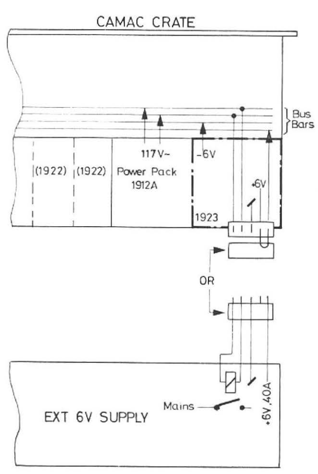
The User Company chose CAMAC because of its extremely good serviceability and ease of operation with PDP-11 computers.

Many additional warehouses will be similarly equipped in the near future.

Ref. no. 12.0003

BORER ELECTRONICS AG offer extra high power facilities for their CAMAC crate. There is a growing tendency amongst large users of CAMAC equipment to fill crates with modules of just one type (e.g. Input Registers) and such assemblies may require considerable power at the +6V level and sometimes some at −6V as well. Often the requirement is for up to 40A at +6V which is beyond the capacity of any combination possible in the Borer 1902A Crate with the widely-used voltage regulators Types 1922 and 1925.

A new voltage regulator module—Type 1923—is now available which is identical to the existing 1925 module (+/−6V at up to 25A) except that it has a heavy-duty connector on its rear panel. By placing a short-circuiting link in this connector the module functions the same as a 1925. An **external** 6V supply can, however, be connected instead. The only modification needed to the external supply is the inclusion of a 117V relay in its mains input which is remotely fed from the crate bus-bars. The relay will ensure that the external supply operates in synchronism with the rest of the crate under turn-on/turn-off/fault conditions. Voltage sensing lines (not shown in the diagram for the sake of clarity) are also extended from the 6V bus-bar to the external supply.



The bus-bars in the Borer Crate 1902A are more than sufficient to handle 40A but users should, however, remember that a 2A per contact limit applies to the PC edge connector. When a crate is operated under such high power conditions, additional cooling is recommended by, for example, installing extraction fans above the CAMAC modules.

Ref. no. 12.0004

NEW PRODUCTS

DATA MODULES
(I/O Transfers and Processing)

Digital Serial Input Modules

Ref. No. 12.0101

High-Speed Quad Scaler

The high-speed Quad Scaler (Model QS100) is a single-width unit that is not only fully compatible with, but exceeds the CERN Microscaler Type 003 specifications. It contains four 24-bit scalers with minimum guaranteed count rate of 100 Mhz. A CAMAC Inhibit gate is common to all sections. An overflow flip-flop acts as a LAM source to interrupt the system controller. An internal switch controls the CAMAC Clear Signal.

By simple serialization the module can be connected for dual 48-bit operation. Serializing switch in position (1+2) allows Sections 1 and 2 to be used in parallel while (1·2) allows Sections 1 and 2 to be used in series. A similar switch is applicable to channels 3 and 4. The QS-100 is intended for use in nuclear physics counting applications where a high degree of compactness is desirable.

Ref. Standard Engineering Corporation

Ref. No. 12.0102

Quad Scaler - 300 MHz with Display

This CAMAC module (3/25) contains 4×24-bit scalers, with a 300 MHz counting frequency. A 7-segment display is provided for each scaler and a LAM signal is generated when the scalers overflow. Mounted on the front panel are the four scaler inputs, a gate input common to the scalers (with lamp), a reset input and a 3-position reset switch (MANUAL/COMPUTER/EXTERNAL).

The CAMAC functions available are:

F(0) A(0, 1, 2, 3)	Read scaler
F(2) A(0, 1, 2, 3)	Read and clear scaler
F(8)	Test LAM
F(9) A(0, 1, 2, 3)	Clear scaler
F(24)	Disable LAM (Mask)
F(25)	Increment scaler
F(26)	Enable LAM
F(27) A(0, 1, 2, 3)	Test LAM status
Q	$[F(0)+F(2)]\ A(0, 1, 2, 3) + F(27).LAM + F(8)\ LAM . \overline{MASK}$
X	For all addressed CAMAC functions accepted by the module

Ref. Schlumberger Instruments & Systèmes

Ref. No. 12.0103

12-Channel, 100 MHz Scaler

The Model 2551 offers twelve independent 100 MHz Scalers in a single-width CAMAC module. Each 50Ω input responds to signals of an amplitude greater than —600 mV and of duration exceeding 5 ns FWHM. Inputs are direct-coupled and thereby independent of rate effects.

The Model 2551 may also be operated in an internal hard-wire-jumper, cascade mode, permitting two adjacent channels to be cascaded for up to 48-bit capability. In the straight 24-bit mode, LAM is generated by the setting of the 24th bit (half scale indication).

Utilizing LRS hybrid circuit design in conjunction with low-power CMOS, the 2551 offers low power dissipation and an unexpectedly high density for 24-bit CAMAC scaler designs, at a price which makes it feasible to utilize just one model for all multiscaling applications. A front-panel inhibit permits common disabling of scaler inputs, and a fast 'clear' input allows full clearing of all scalers within 1 µsec. In addition, all scaler channels respond to F25 and may therefore be easily incremented for remote, on-line testing.

Commands: C, Z, I, Q, X, L,
Function Codes: F0, F2, F8, F9, F24, F25, F26.
Available: February, 1975.

Ref. LeCroy Research Systems S.A.

Digital Parallel Input Modules

Ref. No. 12.0104

Dual High-Speed Gates

This model 2 HSG 2062 is a single-width module with 24 front-panel Lemo connectors, and which offers the user a choice of gate functions. Any ECL IC's may be fitted on request, but the standard range is as follows:

Quad × 2 inputs – OR gate.
Quad × 2 inputs – NOR gate.
Dual × 4 inputs – OR/NOR gate.
Dual clocked RS Flip-Flop.
Dual clocked latch.

The unit provides full CAMAC decoding of two sub-addresses with twenty-four functions each, and when equiped with MECL III's, full NIM signal compatibility.

Ref. SEN Electronique

Ref. No. 12.0105

Fast Coincidence Register

The Coincidence Register (Model CR-6001) is not only very fast but also conserves crate space. It has a high-density packaging and offers 16 complete fast storage channels in a single-width module without exceeding CAMAC power limits.

This coincidence register or pattern unit employs logic channels which seek a coincidence between each of the 16 inputs and a common fast gate input. The unit operates from standard NIM logic levels. It employs ECL integrated circuits to provide coincidence overlap or resolving times under 2 ns.

To eliminate rate effects, the unit is entirely dc coupled and data inputs are designed to offer a high degree of protection against overload and low reflections.

A front-panel reset input is provided for fast clearing of the registers by an external source.

The primary application of this module is in high energy nuclear physics for the pattern recording of hodoscope and spark chamber arrays. Several units may be connected in parallel.

Ref. Standard Engineering Corporation

Ref. No. 12.0106

Status-Interrupt-Module

The Status-Interrupt-Module (C-SI-24) is a single width unit which is used for the processing of a maximum of 24 lines of input information from either one or more external instruments.

Logic and level are bit-separated which can be chosen via internal links. The '0' and '1' state of the module can therefore be defined and the 24 inputs read out directly. When an input sets the state '1' the corresponding status bit is set. This latch register (status register) can be blocked via input 1 and read out and cleared by command.

The required interrupt character is obtained for each of the 24 inputs by clearing or setting the associated masks in the LAM-Mask-Register. For rapid localising of certain interrupts (LAM-sources) one can carry out a selective test by presentation of a bit pattern via the write lines or four LAM-Group-Tests of 6 bits each.

Ref. Wenzel Elektronik

Digital Output Modules

Ref. No. 12.0107

Real-Time Clock

The single-width Real-Time Clock, Model RTC-018, is basically a presettable counter which is fed via a frequency divider and also contains an independent oscillator. Great flexibility is derived from the combination of simple logic elements and a variety of front panel (or Dataway) inputs which can be jumpered to obtain various modes of operation.

The basic operational modes are:

1) A presettable counter; The preset counter of capacity 2^{16} counts when used with the full range 2^{18} of the frequency divider will count from 1 count to 2^{34} counts, in 7 stepped scales.
2) A preset timer; Employing both the clock and the frequency divider, the unit has a time range from 3.8 μ secs to 18.2 hours. Again these times are in 7 stepped ranges.
3) Elapsed-time meter or daytime clock; After a start command, an elapsed time can be measured by reading the counter on the fly and since the counter content can be transferred to the computer as often as desired a daytime clock output is attainable.
4) Clock generator; Feeding the output back to Restart results in a free running clock generator with pulses of 100 nanoseconds duration and clock frequencies in 7 steps from 4 Hz per second to 1 pulse per 65536 seconds (18.2 hours).

Ref. Standard Engineering Corporation

Digital I/O, Peripheral and Instrumentation Interfacing Modules

Ref. No. 12.0108

Universal Input/Output Register

This single-width module Type SPS 2090 is designed to a CERN specification and has the capability of sending and receiving 16-bit data words in parallel. The selection of several modes of data transfer (including handshake) is possible according to the requirement of the external equipment. TTL logic levels are used at input and output. Output signals have open-collector capability of 30 V reverse 40 mA sink.

At each input a 5 mA source from 5 volts is provided. Input and output data transmission is provided independently on two front panel Cannon sockets.

Ref. Nuclear Enterprises

Ref. No. 12.0109

Cassette Interface

The single-width CAMAC module Type JCK 10 has been designed to control a cassette driver type CCK 10 or CCK 11 and conforms to the ECMA 34 standard. The low voltage power required is provided by the crates (19" × 3 U) which contain the cassettes.

The cassette can be read (written) using 8- or 16-bit words (choice according to position of an internal strap).

Data is written on the tape as two 4-bit words with one word on the 'right' side and one word on the 'wrong' side of the tape. This permits checking of read and write and allows the tape to be read in both directions. One 8 bit command register supplies the necessary control parameters. The rewind command carries out all the processes required to position the tape for the first track. Forward and reverse inter record gaps are made automatically.

Ref. Schlumberger Instruments & Systèmes

Ref. No. 12.0110

Interfacing Input Unit

The SPl-CAMAC Source module is a single-width CAMAC module that accepts eight data bits in parallel from peripherals equipped with the standard FACIT-SPl interface, such as paper-tape readers, digital-cassette tape recorders and keyboards.

Handshake control of the data transfer ensures that the operation of the unit is synchronised to the speed of the Source-Device.

The module contains two registers:

ACR – Acceptor Control Register (write only)
ADS – Acceptor Data and Status Register (read only).

Ref. ARSYCOM

Ref. No. 12.0111

Interfacing Output Unit

The SPl-CAMAC Acceptor module is a single-width CAMAC module that transfers eight output data bits in parallel to peripherals, equipped with the standard FACIT-SPl interface, such as paper-tape punches, digital-cassette tape recorders, matrix printers, typewriters, indicator panels and Arsycom 9-track industry-compatible tape systems.

Handshake control of the data transfer ensures that the operation of the unit is synchronised to the speed of the Acceptor-Device.

The module contains three registers:

SCR = Source Control Register (write only)
SSR = Source Status Register (read only)
SDB = Source Data Buffer (write only).

Ref. ARSYCOM

Ref. No. 12.0112

Display Synchronization for European Standard TV Monitors

With Kinetic Systems' new Model 3200E Display Synchronization module, the KSC interactive color display system is now compatible with the European standard 50 Hz, 625-line TV Monitors. This display system is a set of four modules, the Model 3200E Display Synchronization, the Model 3205 Display Timing, the Model 3210 Display Control and the Model 3212 Display Refresh. The system provides both a composite video for black and white TV monitors and an RGB output for color TV monitors. The display refresh memory and character generators are included in the modules. The system can display a matrix of 44 × 24 alphanumeric characters. Each character can be one of seven colors, can be underlined and can be flashed. The characters are generated using a 5 × 7 dot matrix. Bar graphs can be generated with 44 vertical bars, each with a vertical resolution of 1 m 240. The 60 Hz, 525 line version of this system has been operating at a number of installations in the United States. The new Model 3200E makes this system available worldwide.

Ref. Kinetic Systems Corporation

Ref. No. 12.0113

Colour Display Interface

This Type 9062 interface, designed in conjunction with Daresbury Nuclear Physics Laboratories, provides signals for connection into a standard CCTV 625 line, colour monitor. An output is provided for producing a monochrome version of the display on black and white monitors.

The display is composed of a matrix of 2,048 rectangular symbols organised as 64 symbols to a horizontal line by 32 lines. The 2,048 words for a complete display can be stored in the 9061, storage module (see *CAMAC Bulletin*, issue 10, p. 32).

Ref. Nuclear Enterprises

Ref. No. 12.0114

Interface for Multichannel Analysers

A CAMAC control unit (model 5380) has been developed by LABEN for its Series 8000 analysers (models, 8000,8001). The unit enables the user to select the operating modes of the analyser (Stop, Erase, Display, Data In, Data Out) and to perform data transfers between an analyser and a CAMAC system under computer control. The unit is a triple-width CAMAC module provided with one station address (N) and three subaddresses (A) to perform data transfers, command transfers and memory address selection (for remote analyser operation).

Ref. LABEN

Ref. No. 12.0115

Interface for NIM-Standard ADC's

A CAMAC interface, model 5910, has been developed by LABEN to connect its NIM-standard pulse-height converters (models 8215, 8210, 8211, 8212, 8112) and a time-of-flight unit (model 8270) via CAMAC systems to computers.

The interface unit is a single-width CAMAC module.

Ref. LABEN

Digital Handling and Processing Modules

Ref. No. 12.0116

BCD to Binary Converter

The single-width BCD to Binary Converter, Model CD-01 converts a 29-bit binary coded decimal to its equivalent 24-bit binary form. Any such BCD number coded in the 1-2-4-8 binary coded decimal format up to the limiting number, 16,777,216-1, may be converted into the equivalent 24-bit binary number.

Thus a source of BCD data may be monitored, the number converted to binary data and the results placed on the Dataway and fed to a computer.

The conversion time is less than 325 nanoseconds and the result is available both on the Dataway and as signals on the front panel 31-pin Cannon connector. The signal to be converted may be read from the Dataway or from an external source via a 31-pin input connector.

Two modes of operation are available:

- free run in which no control pulses are required and the binary data appearing on the Input data lines is continuously converted and appears at the Output.
- gated, in which the binary Input data appears at both the Output connector and on the Dataway, after an appropriate external strobe on Dataway command.

Ref. Standard Engineering Corporation

Ref. No. 12.0117

Binary to BCD Converter

The single-width Binary to BCD Converter, Model CD-02 converts any 24-bit binary number to its equivalent binary coded decimal form. Up to 24 parallel binary lines may be monitored and their contents converted into the 1-2-4-8 binary coded decimal format, up to the limiting number 16,777,216-1. The conversion time is less than 325 nanoseconds and the result is available both on the Dataway and as signals on the front panel 31-pin Cannon connector. The signal to be converted may be read from the Dataway or from an external source via 31-pin input connector.

Two modes of operation are available:

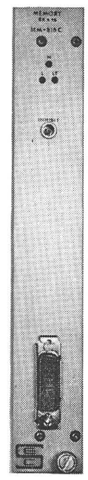
- free run in which no control pulses are required and the binary data appearing on the Input data lines is continuously converted and appears at the Output.
- gated mode in which the binary Input data is converted upon command and will then appear at both the Output connector and on the Dataway.

This unit provides a simple means of obtaining the more intelligible decimal read out from binary measurement on data acquisition systems. For example, the contents of a binary unit such as a scaler may be displayed visually on a line printer, typewriter or visual display unit. Because the convertor operates at high speed there are advantages to its use over the relatively slower software routine.

Ref. Standard Engineering Corporation

Ref. No. 12.0118

Memory Modules



A family of core-memory modules has been designed to meet a wide range of applications requiring a non-volatile memory. For that reason, the module is obtainable in either 16-, or 24-, bit versions. The module is capable of reading or writing data to or from the Dataway interface, and writing data from an external source. A self-contained memory address register can be loaded from the Dataway or reset by the external device. The memory address automatically increments for each read or write operation. The read or write time is one microsecond per word.

A special feature of the module allows information on the Dataway read lines, to be read into the memory when enabled by the P1 line of the Dataway bus. This feature allows data from another module to be written into the memory.

The module is primarily useful as the core memory for a microprocessor located in the same crate. It finds other uses, however, in data compression or when data from the outside world must be read or stored while the computer is out of operation. It is also useful with a programmable controller in order to extend its span of control beyond that of ordinary patch panel control.

Memory modules with a word capacity of 2K, 4K and 8K and a word length of 16-bit and 24-bit respectively are available. (Model numbers: MM 216C, MM416C, MM816C, MM224C, MM424C, MM824C). All memory modules are double-width units.

Ref. Standard Engineering Corporation

Analogue Modules

Ref. No. 12.0119

Fast A to D Converters

Packaged in a double-width module, these ADC's, FADC2068 (dual) and 2067 (single), give conversion times of 2µs for 10bits, and 4.5µs for 12bits. Standard 'Sample and Hold' has an aperture of less than 50ns, and less than 5ns is available as an option.

The units can be interfaced through the CAMAC crate controller in the normal way, or through the SEN DWD2046: in either case the DMA channel can be used. When connected to the DWD however, certain advantages are obtained for the user. Firstly, by setting the Digital Window, all unwanted values are rejected: secondly, the 128 word, 16-bit buffer in the DWD reduces latency time to a minimum by providing block transfer capability.

These ADC's use the successive approximation technique with fixed errors on certain channels. Integral linearity is 1,5 10^{-3}, and differential is

2.5% over 99% of the full scale: the statistical correction table delivered with each module allows this to be improved to better than 0.5% over 100% of the channels.

Ref. SEN Electronique

Ref. No. 12.0120

High-Speed Digitizer

The High-Speed Digitizer, Model SA/D-01 is a single-width unit for digitizing fast 0 to +3V analogue signals. A high speed A to D Converter and a 256-word solid state memory make up the major components of the unit. The A to D converter action is initiated either by Dataway command or by a front panel external pulse. Digital output from the A to D converter is stored in successive locations of the solid state memory until the memory is full whereupon digitizing action is halted and a 'Look-At-Me' is set. Read out of the memory is accomplished either by block transfer or selectively setting the memory address, then reading that particular memory location.

Extremely fast analog signals up to 10MHz rate may be digitized with a resolution of 6 bits. Typical application would include the digitizing of photo multiplier, infra-red detector, laser or other fast time constant devices, and transient waveform analysis signals. Several digitizers may be slaved together by using one unit as a master controller with the other units slaved to the master unit's control signals. A to D conversion rate of the master unit may be controlled at the fixed internal rate or from an external pulse source.

Ref. Standard Engineering Corporation

Ref. No. 12.0121

Solid State Multiplexer

The single width unit, Model MX-016, is a 16-channel high-speed solid-state multiplexer with either manual, random, or sequential channel addressing. By means of patch jumpers on the printed circuit board, this multiplexer may be operated as a 16-channel single ended, or 8-channel differential multiplexer.

The channel address is controlled from the decoded state of a 4-bit counter which is loaded via the Dataway, or incremented by three methods:

1. With function command (F25).
2. Via a front-panel manual push-button.
3. With external pulse via front-panel LEMO connector.

Several multiplexers may be directed to a common output line when the number of signals required to be multiplexed exceeds the capacity of a single module.

Scan Mode

The inputs of interconnected multiplexers may be automatically scanned and sequenced in conjunction with an associated ADC. Each time the first multiplexer receives a scan trigger input pulse, the multiplexer will step to its next successive channel. On reaching its end channel, a 'Next Module' flip-flop is set and the first multiplexer will pass all further scan trigger pulses onto the second multiplexer, and so on until the last multiplexer's full channel count is reached, whereupon a Look-At-Me is generated.

The 'Next Module' flip-flop and the 'LAM' flip-flop may be masked out when the module is used without other multiplexer modules.

Manual Control

For use during the maintenance and system check-out, the MX-016 is equipped with a front panel push-button which will increment the channel number in steps of one. LED indicators on the front panel show the present channel number.

Ref. Standard Engineering Corporation

Ref. No. 12.0122

CPS 2065 CAMAC Controlled Pulse Shaper

The CPS2065 is a single-width unit designed in MECL III technology, and provides fast electronic capabilities under CAMAC Dataway control. There are four PM inputs, four NIM inputs and six NIM outputs: in addition, there is a 'WIDTH' line input/output with adjustable threshold.

The unit can operate in three modes:

- Transparent Mode – NIM signals remain unaffected by PM signals.
- Monostable – the leading edge of any PM pulse generates a new pulse having a width determined by the 'WIDTH' line.
- Bistable – a pulse is generated whose transition to the '1' state is defined by the leading edge of the PM pulse. The subsequent transition to the '0' state is defined by a NIM pulse passing from '0' to '1'.

The following CAMAC functions are available:

F16 A0 at S1, the following are loaded into memory:
W1 – W4. '1' inputs inhibited.
W5 – W6. Modo Mono, Bistable or Transparent.
W7 – W12. Polarity of NIM outputs.
Q Response.

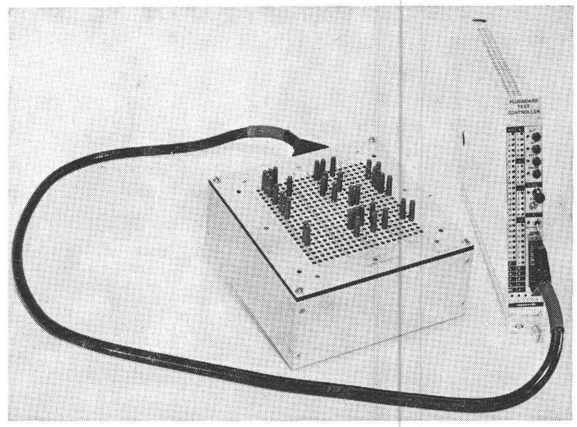
F9 A0 Initialize at S2.

F0 A0 Reads the word on R1-R12.
Q Response.

Ref. SEN Electronique

SYSTEM CONTROL
(Computer Couplers, Controllers and Related Equipment)

Interfaces/Drivers and Controllers



Ref. No. 12.0201

CT 2058 CADET (CERN Type 141)

This single-crate controller for a CAMAC read-only system was originally designed at CERN. Now in production by SEN, the CADET provides an economical method of automatically transferring and recording data containing in up to 19 user modules. When connected with the Print Buffer PB2059, hard copy output can be made on an inexpensive type of printer.

The READ cycle can be set to occur at any desired interval within the dataway timing, and any bit in the system can be selected as a reference to command a Read and display cycle.

The CADET unit may also be used as a manual test facility for a crate. Any unit in the crate can be addressed and the state of the address read from the front-panel display in BCD or binary, 16 or 24 bits.

Ref. SEN Electronique

TEST EQUIPMENT

System Related Test Gear

Ref. No. 12.0301

Single-Crate Test Controller with Program Plugboard

This SPS2048 consists of two units:

1. A double-width CAMAC module which occupies the control station and the adjacent normal station of a CAMAC crate.
2. A diode programming matrix forming the program plugboard.

The plugboard connects to the controller via a 52-way cable and generates 'NAF' commands for execution by the controller. Up to 20 instructions are possible using one plugboard. Up to 5 plugboards, may be linked together to provide a maximum of 100 instructions. In addition to the 'NAF' command the instruction word includes five complementary test options: test absence or presence of Q, X response, L, and conditional or unconditional jump to the 8-bit address specified.

Ref. Nuclear Enterprises

Dataway Related Testers and Displays

Ref. No. 12.0302

Dataway Service Module

The JDS10 (1/25) conforms to CERN specifications reference Laboratory II 73-19 providing necessary service facilities at the dataway level of each CAMAC crate.

The facilities which must be provided by the JDS10 are:

- Programmed check-out of all dataway signal lines with ability to make diagnostics when faults exist;
- Display of logic state of all dataway signal lines including L lines;
- Alarm output for permanently set or noisy dataway lines;
- Internal LAM source set by manual push-button or program control;
- Internal selection for CAMAC address (display on front panel);
- Internal selection for identify code;
- Test points for signals B, S1, S2,
- Simple LAM Grader.

Ref. Schlumberger Instruments & Systèmes

Index to Manufacturer's News and New Products

NEWS

IEC MEETING OF TC 45

Technical Committee No. 45 of the International Electrotechnical Commission (IEC) met in Milan/Rome during the middle two weeks of November 1974. One of its Working Groups (WG3 - Interchangeability) has the task of progressing CAMAC (and NIM) to the status of an IEC recommendation thereby achieving formal recognition of CAMAC as an international standard.

This is a most complicated task and the most appropriate method of reporting on progress is adopted in Fig. 1. This diagram can be understood if one recalls that a document has normally to pass through the various stages of being a Working Group document (WG), progressing to a Secretariat Document (SEC), for comment by National Committees, then a Central Office Document (CO), for National Committees to cast their votes in favour or against it becoming an IEC recommendation (IEC). The status changes typically occur at a clock interval of ONE-YEAR but some documents have been known to have their status unchanged for several clock intervals!

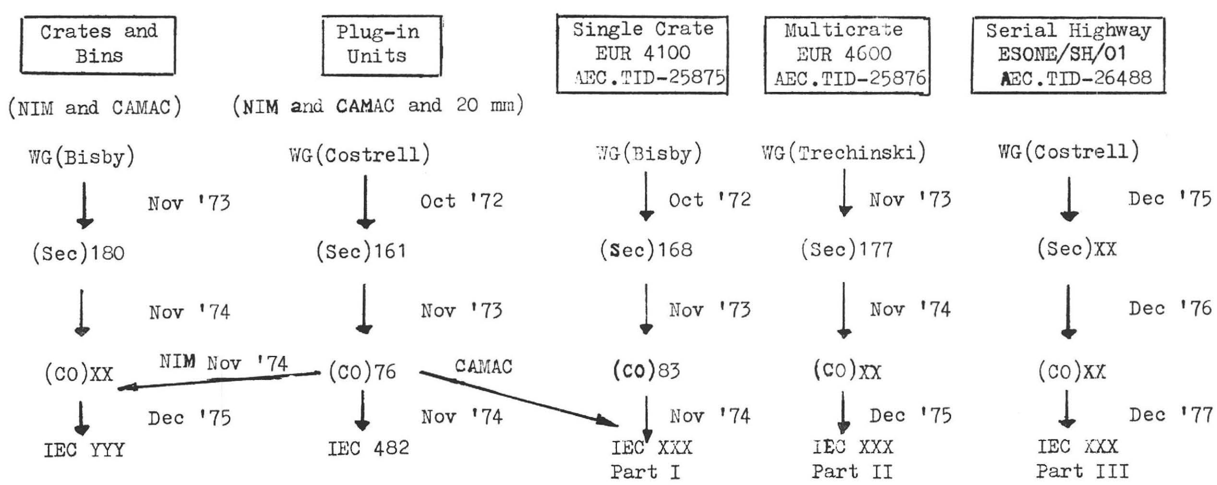


Fig. 1 Current Status of IEC Documentation of CAMAC and NIM

IEC 482 has been published. It refers to plug-in units of NIM, CAMAC and 20mm (USSR) systems. Because IEC XXX part I, when it appears in 1975, will contain the relevant CAMAC information contained in IEC 482 and 45 (SEC) 180, TC 45 have agreed to retain IEC 482 until such time as IEC YYY, devoted entirely to NIM bins and plug-in units, and IEC XXX part I devoted entirely to EUR 4100/TID 25875, appear IEC 482 may then be made obsolete, or incorporated elsewhere by TC 48 (Racks and Panels).

On the basis of this current status it is likely that IEC XXX part I will be available this summer and IEC XXX part II in 1976. Both will be identical to the respective EUR/TID document updated to take in all amendments and additions.

Prior to the Milan meeting, an inadvertent change to the front-panel height of the CAMAC module, in the draft IEC 482, caused an international flutter but this was corrected at the Milan meeting.

PAPER ABSTRACTS TRANSLATIONS

The CAMAC Serial Highway - a functional view
D. L. Abbott

Summary

This paper describes the Serial Highway in terms of the fundamental design parameters of serial systems, such as synchronization and message structure. It is shown that potential applications include non-CAMAC as well as CAMAC environments.

Zusammenfassung

Es wird der serielle Datenweg (Serial Highway) in Hinblick auf die wesentlichen Auslegungsparameter serieller Systeme wie Synchronisation und Nachrichtenstruktur beschrieben. Es wird dargelegt, daß Anwendungsmöglichkeiten sowohl für Nicht-CAMAC als auch für CAMAC Systeme bestehen.

Résumé

Cet exposé décrit l'Interconnexion de branche-série, en termes de paramètres fondamentaux pour la conception de systèmes série, tels que synchonisation et structure des messages. On montre que les applications potentielles comprennent des utilisations non-CAMAC aussi bien que CAMAC.

Riassunto

L'articolo descrive il collegamento serie soffermendosi sui parametri fondamentali di progetto dei sistemi serie, come la sincronizzazione e la struttura del messaggio. Si dimostra che le possibilità di applicazione si estendono tanto ai sistemi CAMAC che non-CAMAC.

Samenvatting

Dit artikel beschrijft de CAMAC Serial Highway. Gewezen wordt op de algemene toepasbaarheid van dit systeem en verder wordt aandacht besteed aan het in de serie-keten opnemen van non-CAMAC apparatuur (data terminals, HP Instrument bus).

Резюме

Описана последовательная магистраль с точки зрения проектированных параметров последовательных систем таких как синхронизация и структура посылок. Показано, что потенциальные применения возникают не только в области применения CAMAC-а.

A CAMAC application in the quality control of high temperature reactor fuel
W. Attwenger and F. Buschbeck

Summary

Special measuring systems using CAMAC have been designed for on-line quality control during the production of coated fuel particles for high temperature nuclear reactors.

Zusammenfassung

Für die 'on-line' Qualitätskontrolle während der Herstellung von beschichteten Brennstoffteilchen für Hochtemperaturreaktoren wurde eine besondere Messeinrichtung entwickelt wofür das CAMAC System Anwendung fand.

Résumé

Des systèmes de mesure spéciaux utilisant CAMAC ont été conçus pour le contrôle de qualité pendant la production de particules de combustible enrobées destinées aux réacteurs nucléaires à haute température.

Riassunto

Sono stati progettati sistemi di misura speciali basati su CAMAC per il controllo di qualità in linea durante la produzione di particelle di combustibile rivestite destinate ai reattori nucleari ad alta temperatura.

Samenvatting

Speciale meetsystemen waarbij gebruik wordt gemaakt van CAMAC werden ontwikkeld voor on-line kwaliteitscontrole bij de produktie van coated fuelparticles voor hoge-temperatuur gas gekoelde kernreactoren.

Резюме

Разработанные специальные измерительные системы для контроля качества он-лайн при производстве деталей топлива для высоко-температурных ядерных реакторов.

A CAMAC-based laboratory computer system
G. P. Westphal

Summary

A CAMAC-based laboratory computer network is described. By sharing a common mass memory this offers distinct advantages over slow and core-consuming single-processor installations. A fast compiler-BASIC, with extensions for CAMAC and real-time, provides a convenient means for interactive experiment control.

Zusammenfassung

Ein auf CAMAC basierendes Laborcomputernetwork wird beschrieben. Mit einem gemeinsamen Massenspeicher bietet dieses System eindeutige Vorteile gegenüber langsamen und speicheraufwendigen Einzelprocessoranlagen. Ein schneller Kompilierer — BASIC — mit Erweiterungen für CAMAC und Echtzeitverarbeitung ist ein geeignetes Mittel zur Steuerung von Experimenten im Dialogverkehr.

Résumé

Description d'un réseau d'ordinateurs de laboratoire basé sur le système CAMAC. L'utilisation en temps partagé d'une mémoire de masse commune, offre de nets avantages par rapport aux installations monoprocesseur lentes et consommatrices de mémoire. Un compilateur rapide, BASIC, équipé d'extensions CAMAC et temps réel, constitue un moyen adéquat pour la commande conversationnelle des expériences.

Riassunto

Si descrive una rete di calcolatori da laboratorio basata sul CAMAC. Utilizzando in comune una memoria di massa si ottengono cosi' particolari vantaggi rispetto agli impianti a singola unità di calcolo, che sono lenti e richiedono una grande capacità di memoria. Un compilatore rapido BASIC, adattato per il CAMAC e per il tempo reale, fornisce un mezzo idoneo per il controllo interattivo degli esperimenti.

Samenvatting

Dit artikel beschrijft een computer netwerk voor laboratorium automatisering. De via CAMAC aan een PDP 11/45 gekoppelde experimenten worden bestuurd met behulp van een multi-user BASIC, voorzien van een uitbreiding ten behoeve van real time CAMAC toepassingen.

Резюме

Описана цепь CAMAC лабораторных ЭВМ. Используя общую массовую память она предлагает чёткие достоинства по сравнении с медленными и нуждающимся в больших памятях одно-процессорными установками. Быстрый компайлер Базика расширеный на CAMAC и реальное время позволяет удобно управлять экспериментом в конверсационном режиме.

Ground Replay Equipment for the Alpha Jet crash-recorder
B. Müller and K. Rosenblatt

Summary

Two Ground Replay Equipments (GRE) have been developed to read data from the crash-recorder of the Alpha Jet after each flight. The equipment is a mobile station, with recorder replay electronics consisting entirely of standard CAMAC modules controlled by a Dornier CAMAC data-processor. Special development was needed only for the software.

Zusammenfassung

Für die Wiedergabe von 'Crash Recorder' Aufzeichnungen des Alpha Jet nach jedem Flug wurden zwei bewegliche Bodenstationen entwickelt. Für den elektronischen Aufbau der Stationen sind ausschliesslich CAMAC Einheiten verwendet worden. Diese werden durch den CAMAC Datenprocessor von Dornier gesteuert. Besondere Entwicklungsarbeiten waren deshalb nur für die Realisierung der Software nötig.

Résumé

Deux stations de restitution au sol (GRE) ont été construites pour la lecture des données fournies par l'enregistreur d'accident de l'Alpha Jet, après chaque vol. Cet équipement est constitué d'une station mobile équipée d'un dispositif électronique de restitution uniquement composé de modules CAMAC normalisés, contrôlés par un processeur CAMAC Dornier. Seul le logiciel a nécessité une étude spéciale.

Riassunto

Sono stati sviluppati due impianti di ascolto al suolo (GRE) per la lettura dei dati dalla "scatola nera" dell'Alpha Jet dopo ciascun volo. Si tratta di una stazione mobile munita di registratore d'ascolto composto esclusivamente da moduli standard CAMAC a azionato da un'unità di calcolo Dornier CAMAC. Sono stati necessari sviluppi particolari soltanto per il software.

Samenvatting

De beschreven twee grondstations werden ontwikkeld om de gegevens van een ALPHA-JET crash-recorder na elke vlucht uit te lezen.
De mobiele stations zijn samengesteld uit standaard CAMAC modules en worden bestuurd door een programmeerbare DORNIER controller.
De benodigde software is opgeslagen in een 1/4 K ROM geheugen.

Резюме

Разработаны две установки для сьема данных из рекордера катастрофы после каждого полёта самолёта Alpha Jet. Устройство является подвижной стацией содержающей стандартные блоки CAMAC управляемые процессором CAMAC фирмы Дорнер. Отдельной разработкой являются лиш только программы.

CAMAC modules for angular shaft-position measurement

Frederick A. Joerger* and Dale W. Zobrist**

Summary

Versatile CAMAC modules have been designed for obtaining position measurements of rotating shafts. Both angular position and the n umber of revolutions are calculated and made available to the Dataway. Each module provides in a si ngle unit all that is needed to couple the transducer to the Dataway.

Zusammenfassung

Vielseitige CAMAC-Moduln sind für Messungen der Position von Drehachsen entwickelt worden. Die Winkelposition und die Zahl der Umdrehungen werden berechnet und dem Datenweg zugänglich gemacht. Jeder Modul weist als einzelne Einheit die Instrumentierung auf, die zur Kopplung des Wandlers mit dem Datenweg notwendig ist.

Résumé

Des modules CAMAC très souples ont été conçus pour mesurer la position d'axes rotatifs. La position angulaire et le nombre des révolutions sont calculés et disponibles sur l'Interconnexion. Chaque module fournit en un seul tiroir tout ce qui est nécessaire pour coupler le transducteur à l'Interconnexion.

Riassunto

Sono stati progettati moduli CAMAC versatili per misurare la posizione degli alberi rotanti. La posizione angolare ed il numero di giri vengono calcolati e trasmessi all'Interconnessione. Ogni modulo in unità singola comprende tutti i dispositivi necessari per accoppiare il trasduttore all'Interconnessione.

Samenvatting

Voor drie soorten aspositiegevers (absolute encoders, synchrotransmitters en incrementele encoders) zijn CAMAC modules ontwikkeld. De hoekstand en het aantal omwentelingen worden bepaald en aan de dataway toegevoerd. Elk moduul bevat de electronica die nodig is om de omzetter aan de dataway te koppelen.

Резюме

Разработанные блоки CAMAC для измерения угловых координат вращающихся валов. Вычисляется угловые координаты как и число оборотов и передается на магистраль. Любой блок содержает всё что нужное для сцепления датчика с магистралой.

A CAMAC branch driver for the PDP-8/E computer

M. Nadachowski* and J. Bundgaard

Summary

This relatively simple branch driver connects a CAMAC Branch Highway to a PDP-8/E computer. The driver occupies three DEC mounting boards, which are inserted directly into the OMNIBUS of the computer.

Zusammenfassung

Dieser vergleichsweize einfache Branch-Treiber verbindet einen vertikalen CAMAC-Datenweg mit einem Rechner PDP-8/E. Der Treiber nimmt drei DEC-Einbauplätze in Anspruch, die sich unmıttelbar im OMNIBUS des Computers befinden.

Résumé

Cette commande de branche relativement simple relie une Interconnexion de Branche CAMAC à un ordinateur PDP-8/E. La commande de Branche occupe trois cartes DEC insérés directement dans l'OMNIBUS de l'ordinateur.

Riassunto

Questo elemento di comando del ramo, relativamente semplice collega il ramo principale CAMAC ad un calcolatore PDP-8/E. L'elemento di comando occupa tre basette di montaggio DEC che vengono inserite direttamente nell'OMNIBUS del calcolatore.

Samenvatting

Deze relatief eenvoudige branch driver verbindt een CAMAC Branch Highway met een PDP-8/E computer.

Резюме

Довольно простой драйвер ветви присоединяет магистраль ветви CAMAC к ЭВМ ПДП-8/Е. Драйвер занимает три монтажные платы DEC включеные прямо в OMNIBUS ЭВМ.

A CAMAC serial driver-receiver

G. Messing*, J. Stolte and E. Kwakkel

Summary

A serial driver-receiver has been developed for controlling remote experiments. The driver-receiver controls a CAMAC Serial Highway loop and contains an interface for the ALPHA-16-LSI-2 minicomputer. The devices connected to the serial loop are adapters to parallel Branch Highways.

Zusammenfassung

Zur Fernsteuerung von Experimenten ist ein serieller Treiber-Empfänger entwickelt worden. Er steuert eine serielle CAMAC-Schleife, und er enthält einen Anschluß an den Kleinrechner ALPHA-16-LSI-2. Bei den mit der seriellen Schleife verbundenen Vorrichtungen handelt es sich um Anschlüsse an parallele vertikale Datenwege (Branch Highways).

Résumé

Un récepteur-commande de branche série a été mis au point pour la commande à distance des expériences. Le récepteur commande de branche contrôle la boucle d'une Interconnexion de branche série CAMAC; il contient une interface pour le mini-ordinateur ALPHA-16-LSI-2. Les dispostifs reliés à la branche série sont des adaptateurs à des Interconnexions de branche parallèles.

Riassunto

E' stata sviluppata un'unità di comando-ricezione serie per controllare esperimenti a distanza. L'unità di comando-ricezione controlla un collegamento serie CAMAC e contiene un'interfaccia per il minicalcolatore ALFA-16 LSI-2. I dispositivi collegati al collegamento serie sono adattatori per collegamenti paralleli del ramo principale.

Samenvatting

De beschreven serial driver-receiver koppelt een CAMAC Serial Highway met een Alpha-16-LSI-2 minicomputer. Serial Branch adapters verbinden de Serial Highway met diverse parallel Branch Highways.

Резюме

Разработан последовательный драйвер-приемник для дистанционного управления экспериментов. Он управляет петелю последовательной магистрали CAMAC и содержает интерфейс ЭВМ Alpha-16-LSI-2. Приборы включенные в петель являются адапторами магистрали параллельной ветви.

CAMAC modules for industrial analog measurement equipment

J. Biri, L. Somlai, Gy Somogyi

Summary

A family of CAMAC modules for analog measurements has been developed as the first step towards meeting the requirements of industrial applications.

Zusammenfassung

Es wird eine Serie von CAMAC Einhetein fqr Analogmessungen beschrieben, welche als eine erste Voraussetzung zur Erfüllung von Erfordernissen für die Verwendung von CAMAC in der Industrie entwickelt wurden.

Résumé

Une famille de modules CAMAC pour mesures analogiques a été développée; elle représente la première étape du développement répondant aux applications industrielles.

Riassunto

E' stata sviluppata una famiglia di moduli CAMAC per misurazioni analogiche quale primo passo verso la risoluzione dei problemi connessi ad applicazioni industriali.

Samenvatting

Met de ontwikkeling van een serie CAMAC-modulen voor het meten van analoge signalen wordt de grondslag gelegd voor een betere aanpassing aan de, in verband met industriële toepassingen te stellen, eisen

Резюме

Разработана семья блоков CAMAC для аналоговых измерений является первым шагом к выполнению требовании промышленных применении.

A fast multi-event digitiser
J. P. Argyle, P. E. Dolley and G. Huxtable

Summary

This time-digitiser, primarily for neutron time-of-flight measurements, is a 5-width CAMAC module. It measures the time intervals between a start pulse and a succession of event pulse with a resolution of 1.25 ns and dead time of 110 ns. It includes an 18-word data buffer.

Zusammenfassung

Dieser vornehmlich für Neutronenflugzeitmessungen bestimmte Impulsgeber ist ein CAMAC-Modul (5 Einheiten breit), der die Zeitintervalle zwischen einem Startimpuls und einer Folge von Ereignisimpulsen mit einem Auflösungsvermögen von 1,25 ns und einer Totzeit von 110 ns mißt. Er enthält einen Datenzwischenpuffer für 18 Wörter.

Résumé

Ce codeur de temps utilisé à l'origine pour les mesures du temps de vol des neutrons, est un module CAMAC 5 unités. Il mesure les intervalles de temps entre une impulsion de départ et une succession d'impulsions-évènement avec un temps de résolution de 1,25 ns et un temps mort de 110 ns. Il contient une mémoire tampon de 18 mots.

Riassunto

Questo convertitore numerico di tempo, impiegato soprattutto per misure del tempo di volo di neutroni, è composto da un modulo CAMAC di 5 unità. Esso misura l'intervallo di tempo fra un impulso di partenza e una successione di impulsi di eventi con una risoluzione di 1,25 ns e un tempo morto di 110 ns e comprende una memoria tampone di 18 parole.

Samenvatting

*Dit 5-eenheden brede CAMAC module, bestemd voor vliegtijdmetingen met neutronen, meet de tijdsintervallen tussen een startpuls en elkaar opvolgende pulsen met een resolutie van 1,25 ns.
De dode tijd bedraagt 110 ns. Verder bevat het moduul een FIFO-buffer, groot 18 woorden (24 bits).*

Резюме

Этот временной кодировщик предназначен для измерении времени прелета нейтронов, является 5-модульным блоком CAMAC. Он измеряет временные интервалы между стартовым импульсом и последовательностью импульсов событий с разрешением 1,25 ns и мёртвым временем 110 ns. Он содержит буфер данных на 18 слов.

X-interrupt CAMAC module for use with Borer 1533 crate controller
I. Török

Summary

A module has been developed to provide interrupts from both X and Q in systems with the Borer Type 1533A crate controller (used with PDP-11 computers).

Zusammenfassung

Für Systeme die mit der Rahmensteuerung Type 1533A von Borer (die in Verbindung mit Rechnern PDP-11 verwended werden) arbeiten, wurde ein Modul entwickelt, der von den X und Q Signalen ein Alarmmeldung ableitet.

Résumé

Construction d'un module générateur d'interruptions à partir de X et de Q, dans des systèmes équipés du contrôleur de châssis Borer de type 1533A (utilisé pour les ordinateurs PDP-11).

Riassunto

E' stato sviluppato un modulo per ottenere interruzioni sia da X che da Q in sistemi con un modulo di controllo Borer Tipo 1533A (utilizzato con i calcolatori PDP-11).

Samenvatting

Dit moduul maakt het gebruik van X en Q interrupts mogelijk in systemen, uitgerust met Borer Type 1533A Crate Controllers (toegepast bij PDP-11 computers).

Резюме

Разработан блок обеспечивающий прерывания от X и Q в системах с контроллером крейта 1533 A фирмы Borer (применяемый в месте с ЭВМ ПДП-11).

CAMAC extension for BASIC 2/3 on the ALPHA-LSI computer
J. L. Visschers and A. ten Hertog

Summary

The BASIC software package for the ALPHA-LSI minicomputer is extended with CAMAC statements. This implementation allows real-time interrupts and is useful for module testing and slow process-control purposes.

Zusammenfassung

Das Programmpalet BASIC für den Kleinrechner ALPHA-LSI wird durch CAMAC-Anweisungen erweitert. Dieser Schritt ermöglicht Echtzeit-Unterbrechungen; ferner wird er für das Testen von Moduln und für langsame Prozeßsteuerungen verwendet

Résumé

Le BASIC du mini-ordinateur ALPHA-LSI a été complété par des instructions CAMAC. Cette addition admet des interruptions en temps réel et elle est utile pour les essais de module et le contrôle de processus lents.

Riassunto

Il package di programmazione BASIC per il minicalcolatore ALFA-LSI e stato ampliato includendovi istruzioni CAMAC. Questa modifica consente interruzioni in tempo reale ed è utile per la prova dei moduli e per controlli di processi lenti.

Samenvatting

Het BASIC software pakket voor de ALPHA-LSI minicomputer is uitgebreid met CAMAC statements. Het pakket kan real-time interrupts (LAM) verwerken en is te gebruiken voor trage regelprocessen en het testen van modulen.

Резюме

Мат-обеспечение Базик для ЭВМ Alpha-LSI расширено коммандами CAMAC. Эта имплементация допускает прерывания в реальном времени и является полезной для проверки блоков и управления медленными процессами.

CAMAC software-driver for real-time system RSX-11D on the PDP-11/40 or 11/45
H. Heer and H. Pohl

Summary

A CAMAC software-driver for the Crate Controller Type 1533A (Borer Electronics) has been developed as an I/O-request-queue managing device-driver in the event-driven RSX-11D real-time system.

Zusammenfassung

Zur Behandlung von Warteschlange mit einer Rahmensteuerung Type 1533A von Borer wurde für das Echtzeitsystem RSX-11D eine CAMAC Software entwickelt.

Résumé

Un segment de programme CAMAC a été mis au point pour le contrôleur de châssis type 1533A (Borer Electronics); il est utilisé comme commande du dispositif de mise en file d'attente de demandes d'entrées-sorties dans le système temps réel RSX-11D.

Riassunto

Un'unità di comando di software CAMAC per il modulo di comando tipo 1533A (Borer Elettronics) è stato sviluppato quale dispositivo di gestione di sequenze di richieste I/O nel sistema in tempo reale RSX-11D comandato da eventi.

Samenvatting

De beschreven CAMAC software driver voor de Borer Crate Controller Type 1533A, is ontwikkeld als device driver passend in het RSX-11D I/O concept.

Резюме

Разработан програмный драйвер для контроллера крейта типа 1533 A (Borer Electronics) в виде драйвера устройств обслуживающего очередь запросов ввода-вывода в системе реального времени RSX-11 D.

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* Obtainable from: Office for Official Publications of the European Communities. Luxembourg, P.O. Box 1003.

** Publications in the more recent CAMAC Bulletin issues are listed on the inside front cover of this issue.

WAS IST CAMAC ?

CAMAC ist ein Vorschriftenwerk für den Entwurf und den Einsatz modularer elektronischer Datenverarbeitungssysteme.

Seine Regeln erlauben die Anwendung einer Standardschnittstelle für den Anschluss von Rechnern an Datenabgabeeinheiten und Befehlsübernahmeeinheiten in on-line Anlagen. Die einheitliche Handhabung und die Kompatibitität von Produkten (Hardware und Software) verschiedenen Ursprungs und für verschiedene Einsatzbereiche wird angeboten und die Ausnutzung der gegebenen Möglichkeiten wird angestrebt.

Arbeitsgruppen des ESONE-Komitees untersuchen weitere Hardware- und Software-Aspekte von Systemen mit Mess- und Steuerfunktionen. Sie halten dabei engen Kontakt mit den zuständigen Arbeitsgruppen des NIM-Komitees der U.S. AEC, mit der Internationalen Elektrotechnischen Kommission (IEC) und mit Arbeitsgruppen der Europäischen CAMAC Vereinigung (ECA).

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WHAT IS CAMAC ?

CAMAC is the designation of rules for the design and use of modular electronic data-handling equipment. The rules offer a standard scheme for interfacing computers to data transducers and actuators in on-line systems. The aim is to encourage common practice and compatibility between products (both hardware and software) from different sources and for uses in different application areas.

Working groups of the ESONE Committee are considering further hardware and software aspects of systems for measurement and control, and maintain close liaison with similar working groups of the U.S. AEC NIM Committee, with the International Electronical Commission and with working groups of the European CAMAC Association (ECA).

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QU'EST-CE QUE CAMAC?

CAMAC désigne un ensemble de règles pour la conception et l'utilisation d'un système électronique modulaire de traitement de l'information. Il définit un modèle standard de connexion des calculateurs aux organes d'acquisition de données et aux organes de commande dans les systèmes en ligne. Son objectif est de promouvoir l'utilisation de techniques communes et d'assurer la compatibilité entre des produits (tant hardware que software) d'origines différentes et utilisables dans différents secteurs d'activités.

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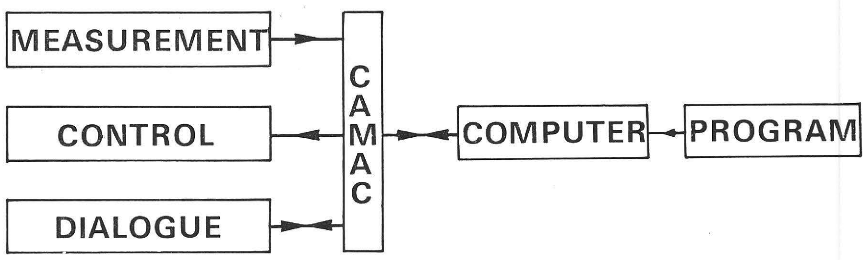

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